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QUARTERLY PROGRESS REPORT

The Air Force Declassification Office concurs in the marked classification
Date 4-30-99 Reviewer 137

DIVISION 6 — DIGITAL COMPUTER (U)

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15 MARCH 1957

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DEPARTMENT OF THE AIR FORCE
HEADQUARTERS ELECTRONIC SYSTEMS DIVISION (AFSC)
HANSCOM AIR FORCE BASE, MASSACHUSETTS 01731

REPLY TO ATTN OF: ALFL (Lincoln Laboratory) 17 Dec 84

SUBJECT: Declassification of Lincoln Laboratory Documents

TO: Mr. M. Wesley/A-109
Security Office
Lincoln Laboratory

1. Reference your letter of 17 Nov 1983 requesting declaassification and public release of MIT Lincoln Laboratory Quarterly Progress Reports issued between June 1952 and December 1958 (see atch 1).

The first major hurdle of this process has been cleared. Attachment 2 authorizes the declassification of the following documents:

"Quarterly Progress Reports - Division 6 - Digital Computer"

15 Jun 1954 (C)-(LL # 1, C315172C)
15 Sep 1954 (C) (LL # 1, C315189C)
15 Sep 1956 (C) (LL # 1, C315208C)
15 Mar 1957 (C) (LL # 1, C315206C) 1714
15 Jun 1957 (C) (LL # 1, C315253C)
15 Sep 1957 (C) (LL # 1, C315254C)
15 Dec 1957 (C) (LL # 1, C315255C)
15 Mar 1958 (C) (LL # 1, C315256C)
15 Jun 1958 (C) (LL # 1, C315257C)
15 Sep 1958 (C) (LL # 1, C315258C)
15 Dec 1958 (C) (LL # 1, C315313C)

The next major hurdle is obtaining public release. This will be done through ESD Public Affairs (Mr. John O'Brien).

ORIGINAL SIGNED BY

THOMAS J. ALPERT, Major, USAF
Chief, ESD Lincoln Laboratory Project Ofc

2 Atch
1. Lincoln Laboratory Ltr, 17 Nov 1983
2. NORAD Ltr, 26 Nov 84

Cy to: D. Murphy/B-107 w/atch
W. Hill/L-339 w/atch

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HEADQUARTERS
NORTH AMERICAN AEROSPACE DEFENSE COMMAND
PETERSON AIR FORCE BASE, COLORADO 80914-5003

REPLY TO ATTN OF J30S

26 NOV 1984

SUBJECT Classification Review "Quarterly Progress Reports"

TO ALFL (Lincoln Laboratory)

1. In response to ALFL letter, 28 Nov 83, the (11) confidential documents titled "Quarterly Progress Reports - Division 6 - Digital Computer" and dated 15 Jun 1954 through 15 Dec 1958 have been reviewed. Recommend the documents be declassified in whole since the sage system computer no longer exists and information contained in the documents no longer has an effect on national security.

2. To officially declassify these, documents, the 416L Security Classification Guide OPR, which is at HQ Sacramento Air Logistics Center, McClellan AFB, CA (MMCM), must be contacted with the recommendation to declassify.

JOHN E. MOORS, LCOL, CF
Ch, At Sensors Division

Memo for Record 14 Dec 84

Talked, by phone, with Ed Smalden, Sacramento ALC/MMCM, McClellan AFB, CA. Based on the recommendation in this letter he considers these documents declassified.

THOMAS J. ALPERT, MAJOR, USAF
CHIEF, ESD LINCOLN LABORATORY PROJECT OFC

Atch 2

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QUARTERLY PROGRESS REPORT

DIVISION 6 – DIGITAL COMPUTER (U)

15 OCT. 63

15 MARCH 1957

ISSUED 4 SEPTEMBER 1957

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LINCOLN LABORATORY LEXINGTON, MASSACHUSETTS

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DIVISION 6 SUMMARY

Division 6, during December 1956, January, and February 1957, had completed assembly testing, adapted to ESS, and delivered on 3 December to Group 64, Package A of the direction center active (DCA) computer program; had Package B ready for delivery by the end of the quarter; carried out 32 system shakedown tests on the Experimental SAGE Sector (ESS); completed tests on Package A at the McGuire Air Force Base; simplified, with the cooperation of the 4620th ADW, the DCA program to the extent that some 35,000 registers of drum storage were saved, thereby eliminating the excessive requirements for drum storage in AN/FSQ's, which developed in the initial writing of the DCA program; had operated all 38 digit-planes of the 256^2 memory with a cycle time of 6.5 μsecs; and continued participation in the preliminary planning of the integration of new weapons into the SAGE System.

Package A of the DCA program was assembly tested, adapted to ESS, and delivered by Group 67 to Group 64 on 3 December 1956 – one month ahead of schedules predicted in June-July 1956 – for the first ESS shakedown test. Package B was ready for delivery by the end of the quarter. At the same time that the packages are turned over to Group 64, they are also delivered to Group 66 for adaptation to and installation at the McGuire direction center. Group 66 completed tests and installation of Package A at McGuire and, by the end of the quarter, were ready to begin on Package B.

ESS system shakedown testing was begun on 3 December 1956. By the end of the quarter, 32 such tests had been conducted on all functions contained in Package A, i.e., radar inputs, manual track detection and initiation, automatic tracking, data simulation, and recording. System performance during these tests has been sufficiently analyzed to conclude that the system conforms in all major respects to specifications for the functions tested and to expect that the testing that will be started in March using Package B will also be successful.

Group 67 and the 4620th ADW completed a review of the operational specifications for a SAGE direction center. The DCA program was consequently simplified resulting in a saving of about 35,000 registers of drum storage. It is estimated that the complete DCA program will now require approximately 92,000 registers and the excessive requirements for drum storage, which developed in the initial writing of the program, have been eliminated. Adequate drum storage is thus insured in AN/FSQ-7's which have 102,000 registers. The workload in assembly testing of the program has also been significantly eased as a result of the improvements made.

All 38 planes (2.5 million bits) of the 256^2 core memory were operating with the TX-0 computer early in the quarter. Cycle time was 6.5 μsecs. A 64-register, single-plane, random-access core memory for storing index numbers and program counts was put in test operation during the quarter. Access time was 0.6 μsecs. An experimental 4-word, 2-digit, model memory, using evaporated metallic films as the memory elements, was constructed during the quarter and demonstrated the possibility of achieving a cycle time of 0.45 μsecs.

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A proposal was submitted for the employment of BOMARC in SAGE and, with some changes, was incorporated into the plan worked out at the ADC employment meeting held in February. Other subjects being studied in the weapons integration effort include the weapons control that can be provided in the McGuire Sector before major revisions are made to the DCA computer program and the non-real-time simulation effort that will be needed to support the weapons integration studies.

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24 July 1957

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TECHNICAL INFORMATION RELEASES

1 December 1956 – 28 February 1957

TIR	Release Date	Material Released
1–191	6 Dec 1956	6M-4534, "Tests of Manual Inputs Systems Design"
1–192	14 Jan 1957	2M-0632, Series A, "South Truro FPS-3 Radar Modifications," dated 11 Dec 1956
1–193	18 Jan 1957	Bell Telephone Laboratory Memorandum, Case 27479-645, "Special Test Equipment for SAGE System Testing," dated 24 Dec 1956
1–194	30 Jan 1957	2M-0633, Revision 1, "Recommendations for Mark X Operation in SAGE," dated 23 Jan 1957

GLOSSARY

AA	antiaircraft
AAOC	AA Operation Center
a-c	alternating current
AD	Air Defense
ADC	AD Command
ADES	AD Engineering Service
ADPE	auxiliary data-processing equipment
ADSOD	Air Defense Systems Operation Division
ADW	Air Defense Wing
AEW	Airborne Early Warning
AF	Air Force
AFB	AF Base
AFCRC	AF Cambridge Research Center
AF IRO	AF Installation Requirements Office
AFMTC	AF Missile Test Center
AGC	automatic gain control
AGET	Advisory Group on Electron Tubes
AI	airborne interceptor
AMC	Air Materiel Command
AMIS	Air Movements Identification Service
APL	Applied Physics Laboratory
AQL	average quality level
ARAACOM	Army Antiaircraft Command
ARDC	Air Research and Development Command
ARTCC	Air Route Traffic Control Center
ASC	Air Situation Coordinator
ASESA	Armed Services Electro-Standards Agency
ASO	Air Surveillance Officer
ASR	automatic send-receive
AST	Air Surveillance Technician
ASTM	American Society for Testing Materials
ATABE	Automatic Target-Battery Evaluation
ATC	Air Training Command
ATCF	ATC Facility
ATO	Air Tactics Officer
ATT	Air Tactics Technician
B-N	bariated-nickel
BOSCO	BOMARC-SAGE Compatibility
BTL	Bell Telephone Laboratories
BSO	Battle Simulation Officer
CAA	Civil Aeronautics Administration
CAT	category
CBS	Columbia Broadcasting System
CC	combat center
CCDC	Cape Cod Direction Center
CDC	call direction code
CCS	Cape Cod System
CER	change evaluation request
C&E	communications and electronics
CHT	Charactron tube
CM	core memory
Codan	Carrier-operated antinoise muting system
CP	Command Post
CPO	command pulse output
CRT	cathode-ray tube
CS	coding specification(s)
DAB	display assignment bit
DACL	Dynamic Analysis and Control Laboratory
d-c	direct-current
DC	direction center
DCA program	the computer program for the active computer of a SAGE direction center
DCO	Design Control Office
DD	digital display
DDG	DD generator
DDL	Division of Defense Laboratories
DDR	digital-data receiver
DDT	digital-data transmitter
DGP	data generation program
DRIP	data-reduction-for-interception program
EADF	Eastern Air Defense Force
ECM	electronic counter-measure
ECP	engineering change procedure
EG&G	Edgerton, Germeshausen & Grier
EMAR	experimental memory address register
ESS	Experimental SAGE Sector
ERA	Electronic Research Associates
FF	flip-flop
FGD	fine-grain data

GLOSSARY (Continued)

FM	frequency modulation
FORX	FGD orientation with Raydist and calibrated Mark X
G/A	ground-to-air
GFI	gap-filler input
GSR	group-selection register
HEC	Hazeltine Electronics Corp.
IBM	International Business Machines Corp.
ID	identification
IFF	identification – friend or foe
INS	interceptor simulator
IPS	initial program specification
IRE	Institute of Radio Engineers
JETEC	Joint Electron Tube Engineering Council
KSR	keyboard send-receive
LPO	Lincoln Project Office
LRI	long-range radar input
LTPS	Lincoln tube process specification
MAR	memory address register
MAT	microalloy transistor
MC	marginal checking
MCD	marginal checking and distribution
MDI	manual data input
MEL	minimum equipment list
M-G	motor-generator
MIL	Military
MOC	Mission Operations Center
MSG	miscellaneous simulation generation
MTC	Memory Test Computer
NAS	Naval Air Station
NET&T	New England Telephone and Telegraph Co.
n-p-n	negative-positive-negative
NRL	Naval Research Laboratory
OB	output buffer
OIST	operator-integration shakedown test
OMR	operational modification(s) request
OPS	operations
OT	Overlap Technician
PCD	power control distribution
PCO	Production Coordination Office
PIUMP	plug-in unit mounting panel
p-n-p	positive-negative-positive
PPI	planned-position indicator
PRF	pulse-repetition frequency
pps	pulses per second
PT	Plotting Technician
QPR	Quarterly Progress Report
RADC	Rome Air Development Center
RAFD	Rome Air Force Depot
RAND	Research and Development Corp.
RC	register containing
R-C	resistance-capacitance
RD	radar data
RECI	Request for Engineering Change and/or Information
RETMA	Radio, Electronics, Television Manufacturers Association
rf	radio frequency
ROTR	receive-only typing reperforator
S&EC	Scientific and Engineering Computation
SAC	Strategic Air Command
SAGE	Semiautomatic Ground Environment
SAHL	semiautomatic height-finder live
SAR	storage address register
SBT	surface-barrier transistor
SD	situation display
SDG	SD generator
SDV	slowed-down video
SIF	selective identification feature

GLOSSARY (Continued)

SIS	SAGE interceptor simulator
SIZ	security identification zone
SC	Signal Corps
SCEL	SC Engineering Laboratory
SO	System Office
SOP	standing operating procedure
SOT	Systems Operations Test
STEP	simulated-tracking evaluation program
SSTP	SAGE System Training Program
SWIG	SAGE Weapons Integration Group
TAPE	Technical Advisory Panel for Electronics
TBS	training and battle simulation
TCAP	Tactical Channel Assignment Panel
TD	track data
TIR	Technical Information Release
TRACALS	Traffic Approach Control and Landing Service
TT	Texas Tower
TWS	track-while-scan
UHF	ultra high frequency
VCM	vibrating-coil magnetometer
VHF	very high frequency
WAD	weapons assignment display
WADC	Wright Air Development Center
WE	Western Electric Co.
WGT	weapons guidance and tracking
WISE	Whirlwind I SAGE Evaluation
WL	warning light
wpm	words per minute
WSEG	Weapons System Evaluation Group
WSPO	Weapons System Project Office
WWI	Whirlwind I
XT	Crosstell, Crosstalk

SYSTEM DESIGN

GROUP 61

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I. SYSTEM DESIGN
GROUP 61

A. SUMMARY

Group 61 has continued to devote its efforts during this quarter to the study of weapons integration with the SAGE System and associated problems.

A proposal has been submitted for the employment of BOMARC in SAGE. With some changes, it was incorporated into the plan worked out at the ADC employment meeting held in February.

The SAGE-Talos Integration Committee completed its report which outlined an effort of about 200 man-months required to complete the integration of Talos with SAGE.

Plans have been made for representatives of each weapon system contractor to work on the integration of its system with SAGE. The studies will be carried out in the Lexington area and should begin early in the next quarter.

Non-real-time simulation of the SAGE tracking and weapons-direction functions is being studied as a means of supporting weapons integration studies, evaluating and acquiring data on performance of computer and air defense functions, and to assist in the development, testing, and checkout of recommended improvements before they are incorporated into the ESS program for final evaluation.

D.R. Israel
R.S. Fallows

B. WEAPONS INTEGRATION

1. BOMARC

The changes to operational and mathematical specifications, necessary for initial BOMARC integration, have been outlined. A method of employing BOMARC, using the SAGE System, has been proposed by Group 61 and Boeing for review by all organizations concerned.* The proposal includes the following principal features:

(a) A list of operational procedures for SAGE direction center personnel for the use of a one-range missile with two choices of warhead

(b) Provision for each direction center to launch missiles from four BOMARC squadrons within or near its sector boundary

(c) Use of BOMARC SIF replies for tracking

(d) Guidance command, which will be computed on an average of once every 15 seconds with the provision that it can be computed at any 5-second interval when needed.

At the ADC employment meeting on BOMARC, held the week of 18 February 1957, the Group 61 and Boeing plan was adopted as the ADC Employment Plan with the following differences:

(e) No provision will be made for command destruction of the missile from the ground

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*Israel, D.R., and Anderson, H.E., "Proposed Initial SAGE/BOMARC Tactical Capability," MIT Lincoln Laboratory Report 6M-4890 (13 February 1957).

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(f) The computer program should be written so that some BOMARC capability is available even if single-pulse Mark X replies must be used

(g) Some capability should exist even if the separate BOMARC ground-to-air transmitter is not available.

Group 61 and Boeing will now proceed to detail the approved employment plan.

2. Talos

The SAGE-Talos Integration Committee met at Johns Hopkins University, Applied Physics Laboratory, in December. This meeting included representatives from Hq. ADC, 4620th ADW, and ARDC Det. 1, in addition to the regular RCA, APL, IBM, ADES, and Lincoln members of the committee.

The committee's report was presented at the meeting and outlined an effort of about 200 man-months that will be needed to complete the integration of Talos with SAGE. RCA has expressed willingness to accept a suitable contract for the work involved and ARDC will attempt to negotiate such a contract. However, responsibility for Talos is being transferred to the Army, whose plans for the weapon are unknown and no information on operational dates is available. No work on an interim system has been contemplated.

3. Manned Interceptors

The Air Force proposed, at a meeting at Wright Field in January, that each interceptor weapons system contractor, whose aircraft will be used in SAGE, assign between 5 and 15 people to work on the integration of their system with SAGE. A steering committee, consisting of one man from each participating organization, will provide technical guidance to the whole group. Studies will be carried on in the Lexington area and work should begin early in the next quarter.

C. WEAPONS CAPABILITY STUDY

Representatives of Group 61, Group 67, RAND, and the 4620th ADW reviewed the weapons control that can be provided in the McGuire SAGE Sector before major revisions are made to the computer program. The study resulted in recommendations for a simple automatic assignment of hostile tracks to the AN/FSG-1 Missile Master for engagement, and some minor modifications of control facilities to provide more effective use of manned interceptors.

D. NON-REAL-TIME SIMULATION OF SAGE FUNCTIONS

Group 61 is planning a non-real-time simulation of the SAGE tracking and weapons direction functions. This simulation would have the following major uses:

(1) To aid in supporting studies for weapons integration tasks

(2) To evaluate the performance of computer functions in both existing and future computer programs

(3) To acquire data on performance of certain air defense functions, e.g., determine the desirable types of attacks to be made by specific interceptors with specific weapons against various bomber types and speeds

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(4) To assist in the development, testing, and checkout of improvement techniques before they are incorporated into the ESS for final evaluation.

A committee consisting of representatives from Lincoln, RAND, and IBM has been proposed for conducting this simulation effort.

In an attempt to obtain concrete data on specific problems related to SAGE tracking accuracy, particularly performance when the target makes a 90° turn, the STEP and DRIP simulation programs are being used on the Memory Test Computer. Plans call for the analysis of 192 combinations of speed, maneuverability, blip-scan, and noise parameters of tracks making these 90° turns. About a third of these combinations were completed at the end of the quarter.

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E. SIF

The problems of SAGE-SIF compatibility were discussed at a meeting at ADES, N.Y., on 15 January 1957 by representatives from USAF, AFCRC, RADC, WADC, BTL, ADES, Burroughs, and Lincoln. ADC is planning to hold an employment meeting for SIF in Rome, N.Y., sometime in April. In preparation for this meeting, Group 61 is studying various methods of employing SIF in SAGE. When a comprehensive employment plan is issued, equipment designs and program specifications can be established.

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ESS INSTALLATION

GROUP 62

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II. ESS INSTALLATION
GROUP 62

A. SUMMARY

Group 62 during this quarter conducted 17 ESS subsystem tests on height finders and radar inputs and continued the installation and maintenance of the equipment in the ESS direction center (Building F, Lexington). For the first time the Bath height-finder subsystem was experimentally operated with the ESS operators and computer programs being tested by Group 64.

All 17 subsystem tests of ESS height finders and radar inputs this quarter were conducted using the XD-1 computer and Bath, South Truro, or Montauk radar sites. Error-rate tests performed on the height-finder subsystem, using XD-1, showed approximately 96 per cent agreement between heights originally recorded at the computer and those received in replies from Bath. This agreement compares favorably with the 97 per cent agreement received from South Truro during the previous quarter when WWI was used.

For the first time, integration of the Bath height-finder subsystem with other parts of the ESS was attempted. The DCA program and ESS operators were used to record and process the information provided by the subsystem. Requests for heights, ranges, and azimuths were radioed from the Bath site to random aircraft, in the area at the time, for checking the accuracy of the system. All heights contained in the 52 replies received from the aircraft agreed satisfactorily with those that were indicated by the subsystem.

The 14-channel Ampex tape recorder for recording phone-line data in ESS has been supplemented by a second one borrowed from IBM. Ampex has a new design available, the FR-100, and two of these machines have been ordered for permanent installation in Building F.

XD-1 computer performance during this quarter indicated increased reliability of the central computer system, but the over-all figures remain the same due to the increase of display system troubles picked up as a result of the start of ESS shakedown testing.

J. A. O'Brien
W. J. Canty
R. S. Fallows

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B. ESS SUBSYSTEMS

1. Radar-Inputs Test Team

A total of 17 tests were performed on ESS subsystems during the quarter. Eight height-finder error-rate tests and eight radar-inputs test-pattern tests were conducted using the XD-1 computer and Bath, South Truro, or Montauk height-finder radars. In addition, a special test using the height-request generator and height-reply monitor in Building B at Lexington was run to determine the accuracy with which the radar antenna slewed to a requested position. The single-track tracking program was subjected to a four-day series of tests with the objective of correcting program errors.

a. Height-Finder Error-Rate Tests

In error-rate tests performed on ESS height-finder subsystems, the computer sends a request containing an arbitrary "old" height, through the AN/FST-2, to a height finder. Since the

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height-finder is not changed in any way, the "new" height contained in its reply to the computer should be the same as that in the request.

The high percentage of exact comparisons between height requests and height replies for the three months ending 28 February 1957, using XD-1, was 96 per cent from the Bath site. This percentage compares favorably with the 97.5 per cent from South Truro, using WWI, for the like period ending 30 November 1956. Little worthwhile data was received from South Truro, where AN/FST-2 equipment was being installed throughout the quarter. Difficulty with Montauk returns was caused by input parity alarms on the Montauk AN/FST-2. Near the end of the quarter the trouble was traced to the DDR at Montauk.

The following results of the test conducted on 21 February 1957 are generally representative of the eight error-rate tests performed on ESS height-finder subsystems during the quarter:

Height Comparisons (total number of requests: 81)

	Montauk	S. Truro	Bath
exact	1%	46%	96%
"no replies"	90%	50%	4%
wrong replies	9%	4%	
total number of replies received	80	79	81

Goal: 99% exact

Range and azimuth were also compared on all height requests to Bath with these results:

Range Comparisons

81% centered within −2, ±1 naut. miles of range sent
94% centered within −2, ±2 naut. miles of range sent

Goal: 90% centered within −2, ±1 naut. miles

Azimuth Comparisons

80% within ±1°
96% within ±2°

Goal: 90% within ±1°

b. Height-Finder Integration with ESS

The height-finder subsystem was tested with other parts of the ESS system on 28 February 1957 using the DCA program for the first time, simulated tracking data, and one Bath height-finder radar. Height requests were radioed to random aircraft in the area at the time to check the accuracy of the system; replies were received from 52 such random "targets" and every height they reported agreed satisfactorily with those contained in the request. Adequate range and azimuth data were included in only 21 of the replies received. These 21 were compared and analysis indicated that:

71 per cent of the ranges were centered within −2, ±1 naut. miles.
76 per cent were centered within −2, ±2 naut. miles of range requested.
43 per cent of the azimuths were within ±1° and 71 per cent were within ±2°.

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Results of this first integrated test of a subsystem with other parts of the whole ESS system, including the air defense computer program and ESS operators, were encouraging.

c. Radar-Inputs Test-Pattern Tests

Eight test-pattern tests were conducted on the long-range radar input (LRI) subsystems. The equipment changes in process at South Truro reduced the quality of data received from that site. Patterns from Bath and Montauk, as received at the LRI monitor, were generally good. Efforts are being made to correct the program and equipment malfunctions to bring the results of this test up to specifications.

The last test-pattern test of the quarter was conducted on 14 February 1957. General results of this test were as follows:

Montauk was operating more accurately than either Bath or South Truro. A point-by-point analysis of the data from the tape record showed that the ranges of 947 of 951 points were exactly right; 406 of 950 were exactly right in azimuth, 539 were within acceptable azimuth limits (+4 and −2 units), and 5 were unacceptable. Four of these five were associated with the range errors.

Throughout the test there was equipment trouble with the Bath and South Truro subsystems. The South Truro range received was either 268 or 396 range units instead of the 397 of the correct pattern. From Bath, 396 or 398 range units were usually indicated.

d. Special Height Request and Reply Test

Height-finder subsystems of the SAGE sectors will be subjected to a relatively simple test described in paragraph 3.02 of the test specification covering height-finder subsystems. A series of 31 specific words is sent to the radar sites and the azimuth to which the radar antenna slews shall be within ±1° of the azimuth sent. This test was conducted using Montauk, Bath and South Truro radars.

Equipment trouble at Montauk prevented processing of our request by the AN/FST-2. Six of the 31 azimuths noted at Bath were in error by more than ±1° and South Truro reported comparable results. Since this was a special test on an ESS subsystem, the points in question were not further tested.

e. Single-Track Tracking Program

Efforts to correct this test program, which is used in ESS subsystem testing, have continued. The height-request portion of the program was incorporated during February and operated well with Bath, but a combination of subsystem equipment and program errors caused poor results from Montauk and South Truro.

f. SAGE Subsystems

Testing by Western Electric of the subsystems of the first SAGE direction center, McGuire, was started during the quarter. The P-site at Benton, Pennsylvania, started operation the week of 4 February 1957. The gap fillers at Gibbsboro, Manorville, and Chilmark have also, at times, been feeding data to the direction center, but not yet enough on which to base an evaluation.

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2. Changes to Teletypewriter Network for ESS

A recent investigation revealed that certain cancellations and reassignments of teletypewriter circuits connecting Building F with radar sites and air bases would be desirable in the interests of economy. The recommended changes are summarized as follows:

(a) reassign inactive ESS circuits for use with the Cape Cod System (applies to Hanscom, Weymouth, Otis, and Westover)

(b) cancel circuits which can be reinstalled when needed on one month's notice (applies to Montauk and Suffolk)

(c) cancel certain other circuits because they are not needed now

(d) keep the remaining circuits for present or near-future use.

3. Keyboard Check Program for XD-1

A computer program for testing keyboards of XD-1 consoles has been brought up to date after substantial revision and correction to allow for the many circuit changes introduced during the past year. The program was verified with the cooperation of IBM in February and turned over to them on the 18th of that month. A few remaining changes to allow for previous wiring alterations will be made by IBM. Meanwhile, the program is being used successfully.

4. XD-1 Reliability

XD-1 operation and reliability for this quarter, measured over one-week periods, are summarized as follows:

Scheduled Computer Hours	1076.95
Interrupting incidents	459
Hours lost	122.11
Per cent good time	88.5
Mean time between failures (in hours)	2.08

The reliability of the central computer, memory, and drums has increased during this quarter through more effective use of the marginal checking system. Of all pluggable units removed from the system because of deteriorating components, the proportion removed as a result of marginal checking has increased from about 50 per cent to about 85 per cent. Use of the display system increased sharply when the ESS shakedown tests began early in December and the numerous failures of this system, although mostly minor in nature, have contributed to a reduction in over-all reliability as indicated in the above summary. The card readers and the tape system also caused many machine failures before the troubles, intermittent in nature, were located. A change in the timing of the card readers made them more tolerant of cards punched slightly out of registration, and an intermittent connector was finally found which explained many of the failures in the tape system.

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C. CIRCUIT SUPPORT

1. Tape Recorders for XD-1

Phone-line tape recorders (Ampex 14-channel) are used in XD-1 primarily for storing raw radar data for later use in simulated tests. A secondary function is that of supplying special test patterns for routine maintenance of computer input and output circuits and peripheral equipment.

During this quarter the single Ampex 3418 which has been performing these functions was supplemented by a second one borrowed from IBM. In addition, two Ampex machines of new design, the FR-100, were ordered for permanent installation.

Concurrently, tests at Lincoln Laboratory, performed in the presence of Ampex representatives, demonstrated that the speed of 30" per second, now used on all of the above recorders, could be reduced to 15" per second with no loss of quality. If incorporated in the machines presently in use, the lower speed would reduce tape handling and permit storage of twice as much data. This modification will be incorporated in the FR-100 and all recorders subsequently ordered.

2. Probe System for XD-1

A probe system* that will enable computer maintenance personnel to efficiently maintain and trouble-shoot the computer from the maintenance console was in its last stages of testing at the end of this quarter. Sixty 200-foot probe cables, four probe guns, an oscilloscope, and a maintenance console patch panel for the probe system have been installed. More computer time is needed to complete checkout tests.

3. Utility Ties at McGuire Air Force Base

An Air Force directive calling for the elimination of utility power ties to the direction center at the McGuire AFB has resulted in a joint recommendation by Lincoln Laboratory, IBM, and WE that the reliability and flexibility designed into the system require either the present utility ties or two additional diesel-driven generators as alternative power.

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D. DESIGN CONTROL OFFICE

1. New Area Discriminator Design for XD-1

On 12 February the details of an improved area discriminator (AD) for XD-1 consoles were released in 6M-4905. A summary of this paper follows:

An AD is a device mounted on a situation display console to gate radar data or track information to be sent to the manual input element. Its function is to enable an operator to mask certain areas of the display for examination elsewhere in the direction center.

*Quarterly Progress Reports, Division 6, Lincoln Laboratory, M.I.T., 15 March through 15 December 1956, Section II.

GROUP 62

The present AD on XD-1 consoles has the following disadvantages:

(a) The post that supports the photomultiplier signal-detector interferes with the operator's view of the display and with his hand movements.

(b) The adjustments of the optical parts of the device are extremely critical, and are quite likely to be disturbed by accidental bumping, or by merely leaning on the console shelf to which the post is attached.

(c) The operator does not see the map, nor does the photomultiplier see the display, with satisfactory clarity.

For these reasons, Lincoln Laboratory, with help from IBM, has redesigned the AD as follows:

(d) The support for the AD head has been attached to the top of the console above the display scope, to eliminate obstruction to the sight and movement of the operator.

(e) The new location of the head lessens the likelihood of accidental bumping.

(f) The sensitivity of the photomultiplier has been increased by eliminating the dichroic mirror.

(g) Black light from the AD head makes the display tube luminous, enabling the operator to see his map clearly as a shadow against the brighter background.

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ADVANCE DEVELOPMENT

GROUP 63

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III. ADVANCE DEVELOPMENT
GROUP 63

A. SUMMARY

All 38 digit-planes of the 256 × 256 × 38 memory (2.5 million bits) were operating with a cycle time of 6.5 μsec with the TX-0 computer early in the quarter. The 64-register index memory (0.6 μsec access time) which stores the index numbers and program counts for the TX-2 computer has been placed in test operation. A 4-word, 2-digit, model memory using thin films has been constructed and has demonstrated the possibility of achieving a cycle time of 0.45 μsec.

New ceramic materials are being studied for applications such as:

Microwave Ferrites – a low-power, L-band isolator with 70:1 reverse-to-forward loss ratio has been built.

Thermistors – controlled processing has yielded experimental thermistors with room temperature resistances of from 250 to 3000 ohms and high temperature resistances of from 0.2 to 0.4 ohms.

Memory Cores – lower-drive cores appear possible as a result of grain-size control using CaO (calcium oxide) flux and specified firing temperatures.

More of the basic characteristics of magnetic materials have been determined through the use of X-ray analysis equipment, a refined vibrating-coil magnetometer, and a new hysteresis-loop tester, all of which were either designed and built or modified in the laboratory. These studies included investigations of magnetic properties at temperatures only a few degrees above absolute zero.

The final design of the display system for TX-2 has been completed. It was developed on the basis of several months of successful operation of a prototype system in TX-0.

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B. MAGNETIC MATERIALS

1. Introduction

All memory cores required for Lincoln Laboratory computers have been produced and the section is again concentrating on the research and development of new magnetic materials. Our strength in research-directed people has increased. For example, the uniformity and control of thin metallic films of nickel-iron alloy will be studied by two new people, one a specialist in high-vacuum techniques (about 10^{-8} to 10^{-10} mm of Hg) and the other skilled in spectrophotometric analysis. The study of fundamental measurements, formerly carried on by one man, has been strengthened by another. Together these two people have considerably improved the sensitivity and flexibility of the vibrating-coil magnetometer and will take extensive measurements on this equipment during the next quarter.

In the ceramics laboratory an almost completely new group of technicians under a relatively inexperienced staff member has been able to meet all production commitments and has branched into the following new areas of interest: microwave ferrites, thermistors, and filter ferrites.

2. Ceramics

a. Memory-Core Production

Production of the small 50-30 mil cores for the transistor-driven memory in TX-2 has been completed. There are now 615,000 pressed, fired, untested cores on hand.

b. Microwave Ferrites

An investigation of the microwave properties of certain ferrites in the $MgO\text{-}Mn_2O_3 - Fe_2O_3$ system has been continued. With one of these compositions, Group 35 has built an L-band isolator with a 70:1 reverse-to-forward loss ratio. The best that has been attained with commercially available ferrites is 11:1. The isolator is expected to be limited to low powers, since the Curie temperature is only 100°C.

The new garnet-type material, $Y_3Fe_2(FeO_4)_3$, has also been prepared. Considerable work is yet required to learn how to make this material with greater density. Unless the body has nearly the maximum theoretical density, local internal fields broaden the resonance line width, $(\Delta H)^2$. These materials are also being supplied to Group 36 for possible use in coaxial high-frequency (several hundred megacycles) phase shifters.

c. Thermistors

Group 62 needs a thermistor with a high resistance (>250 ohms) at room temperature and a low resistance (<0.1 ohms) at 200°C for a circuit which will protect the filaments of certain vacuum tubes from thermal overload and so prolong their life. The thermistor must also have a relatively slow rate of heating (>90 secs) to allow tube filaments time to warm up without exceeding their rated currents. During this quarter, a series of experimental materials has been proposed and initiated to test the hypothesis that the source of thermistor action is a martensitic transformation from tetragonal to cubic symmetry in spinel-type lattices containing Mn^{+++}, Ni^{++}, Cu^{++}, Cr^{++}, or perhaps In^{+++} ions. By controlling the number of these critical ions in the B-sites of the spinel lattice, it is possible to control the temperature at which the transformation occurs. Since the materials are semiconductors, the phase change is accompanied by a marked change in electrical conductivity which alters the magnitude of the energy gap between the valence and conduction bands in the material. Initial experiments have been encouraging: The room-temperature resistivity has been successfully varied from 250 to 3000 ohms with a high-temperature resistance of 0.2 to 0.4 ohms. During the next quarter an attempt will be made to improve the thermistor contacts and thus, it is hoped, reduce the high-temperature resistance.

d. Experimental Ferrites

In order to investigate the electromagnetic properties of a ferrite as a function of grain size, various fluxes were tested which would permit the growth of large grains at temperatures below 1500°C and, at the same time, permit the chemistry to remain constant for a considerable range of firing temperatures. The fluxes studied were CaO, V_2O_5, and B_2O_3. Small additions (~1 to 2 per cent) of CaO were found to be the most satisfactory. A series of cores of varying grain size, all other properties being kept constant, is being prepared.

It is anticipated that considerable use in transistor circuits could be made of lower-drive, slightly slower switching memory cores. A series of magnesium, manganese ferrites with additions of ZnO is being prepared for this purpose.

3. Testing

Testing activities have been focused on the following projects this quarter: A hysteresis-loop tester for the evaporated, magnetic films; a semiautomatic core handler for testing the smaller (50-30 mil), as well as the standard (80-50 mil) cores; and measurements of temperature-frequency characteristics.

a. Hysteresis-Loop Tester

A hysteresis-loop tester for thin films was built which is capable of measuring both rotational and wall coercivities. Evaporated films can be placed in a uniform field (provided by a pair of Helmholtz coils) and rotated at will; a second pair of Helmholtz coils is also available to provide a transverse uniform field for use in studying the rotational coercive force. During the next quarter a third, much larger pair, of Helmholtz coils will be provided to buck out the component of the earth's magnetic field which is in the plane of the film.

b. Core Handler

The building of a core handler for testing the 50-30 mil cores has proved to be difficult. Several different schemes have been tried for improving the feed of the small cores and the testing probe. Each setup has worked well initially, but has deteriorated after testing a few thousand cores. The experience has guided the design of a new model which is expected to eliminate the difficulties. Once the semiautomatic handler is operating satisfactorily, a completely automatic setup is a matter of adaptation.

c. Temperature-Frequency Measurements

A series of temperature-frequency characteristics was measured on both the standard memory composition and on a zinc-containing composition with considerably lower Curie temperature. Satisfactory operation of the zinc-containing composition at 500 kc per second is attributed to its lower hysteresis losses.

4. New Magnetic Materials

a. The System $Li_x^{+}Ni_{1-2x}^{++}Ni_x^{+++}O$

X-ray analysis shows that, for values of x in the range $0 \leqslant x \leqslant 0.325$, this material crystallizes with the cubic rock-salt structure of pure NiO. For the range $0.325 \leqslant x \leqslant 0.5$, a rhombohedral distortion of the lattice is observed. The magnitude of the distortion is represented by a change in the value of the angle at a corner of the original cube from 90° to 88°54'. The corresponding rhombohedral angle, α, decreases by 8' of arc while x changes from 0.325 to 0.5. The distortion of the cubic cell is so small that the rhombohedral phase may be considered to have a pseudocubic unit cell, the dimensions of which vary continuously with the true cell of the cubic phase. The length of the unit-cell edge for pure NiO is a_o = 4.177 Å and decreases almost linearly to 4.080 Å for $Li_{0.48}^{+}Ni_{0.04}^{++}Ni_{0.48}^{+++}O$. The volume of the true unit cell varies linearly

from 72.877 $Å^3$ for NiO to 67.866 $Å^3$ (here we must consider twice the volume of the rhombohedral cell) for $Li^{+}_{0.48}Ni^{++}_{0.04}Ni^{+++}_{0.48}O$.

A significant magnetic moment is observed in this system through the range of compositions with a rhombohedral structure. The maximum saturation moment, 0.3 μ_B per molecule, is observed for a value of x = 0.42. The gram magnetization here is approximately one-half that of pure nickel. The distortion of the crystal lattice and the appearance of a net magnetic moment appear to result from an ordering of the lithium and nickel ions, which occurs for values of x greater than 0.325. A theoretical analysis, which assumes ordering of Li^{+}, Ni^{+++} ions between alternate (111) planes, which couple antiparallel to one another, is capable of explaining the data, provided: (1) a nickel ion has at least two near-neighbor ions on its simple cubic cation sublattice, which are also nickel ions if H is coupled magnetically to the lattice; (2) the ordering of Li^{+} and Ni^{+++} between alternate (111) planes is not complete.

For values of x from 0 to 0.325, preparation of samples is easily accomplished by igniting NiO with the stoichiometric quantity of Li_2CO_3. The rhombohedral phases are more difficult to prepare. $Li^{+}_{0.48}Ni^{++}_{0.04}Ni^{+++}_{0.48}O$ was prepared by fusing NiO with an excess of Li_2O_2, separating the reaction product, and fusing it a second time with Li_2O_2.

b. Additions of Rare Earths to Perovskite-Type Compounds

Nickel oxide reacts with lanthanum oxide at 800°C to form a lanthanum nickel oxide, with a perovskite-like structure. The employment of a sodium carbonate flux in the preparation makes it possible to use lower temperatures and results in clearer X-ray patterns. Solutions containing 500 ppm of dissolved lanthanum nickel oxide were found to contain 3 ppm of sodium. Calculations based on X-ray data show that $LaNiO_3$, belongs to a space group D3d (5) – R3m with two formula weights per unit cell. The dimensions of the rhombohedral pseudocell are a = 7.676 Å, α = 90°43'. The dimensions of the primitive rhombohedral cell are a = 5.461 Å, α = 60°49'. The hexagonal form of this cell has the following dimensions: a = 5.456 Å, c = 13.122 Å. Chemical analysis and determination of the number of "molecules" per unit cell indicate that the formula is $LaNiO_3$.

When mixtures of neodymium oxide and nickel oxide, in a mole ratio of 1:1 were treated by the same procedure used to prepare $LaNiO_3$, a different structure was obtained in addition to excess NiO. A single phase formed whose composition may vary between $Nd_{1.67}Ni^{++}_{0.72}Ni^{+++}_{0.41}O_{3.84}$ and $Nd_{1.75}Ni^{++}_{0.57}Ni^{+++}_{0.43}O_{3.84}$. An increase in the ratio Nd:Ni results in the formation of more trivalent nickel. Solutions containing 500 ppm of dissolved neodymium nickel oxide were found to contain 4 ppm of sodium. X-ray diffraction patterns of this phase were taken with filtered iron radiation. The patterns were rather poor; lines were generally broad and low in intensity. Samples of both compositions $Nd_{1.67}Ni^{++}_{0.72}Ni^{+++}_{0.41}O_{3.84}$ and $Nd_{1.75}Ni^{++}_{0.57}Ni^{+++}_{0.43}O_{3.84}$ gave essentially the same pattern, although a very slight shift of the lines was observed. With the exception of one very weak line at 2Θ = 31.2°, all the lines of these patterns out to 2Θ = 75° could be indexed satisfactorily on the basis of a monoclinic unit cell with a = 3.92 Å, b = 6.16 Å, c = 3.77 Å, and β = 92.4°.

Lanthanum cobalt oxide ($LaCoO_3$), containing trivalent cobalt, was prepared and its structure determined by X-ray analysis. The dimensions of the rhombohedral pseudocell are a = 7.64 ± 0.02, α = 90°42'. The dimensions of the primitive rhombohedral cell are α_p = 60°48', a_p = 5.436 Å. The hexagonal form of this cell has the following dimensions: a = 5.424 Å, c = 13.068 Å. Lanthanum rhodium oxide, containing trivalent rhodium, was prepared by heating an intimate mixture of

lanthanum oxide and rhodium oxide at 1100°C for 72 hours. Lanthanum rhodium oxide is a distorted perovskite belonging to the space group D2h (16)-pbnm of the orthorhombic system. The lattice constants are a = 5.524 Å, b = 5.679 Å, c = 7.900 Å.

5. Fundamental Measurements

a. Refinement of the Vibrating-Coil Magnetometer

(1) Circuits: The electronic circuitry on the output side of the vibrating coil has been completely altered to improve the sensitivity and ease of measurements. The new input circuit permits separate adjustment of both the phase and amplitude of the signals emanating from each of the vibrating coils. The new phase-sensitive detector provides greater amplification and an improved signal-to-noise ratio. The peaked amplifier was discussed in the previous Quarterly Progress Report.

(2) Auxiliary Equipment: (a) The vacuum system which is to be used with the helium dewar to achieve temperatures below 4.2°K has been installed, and preliminary tests indicate satisfactory operation. (b) Various sample holders have been completed. Those designed for magnetostriction and crystalline anisotropy measurements have been used successfully during the last period. A new Teflon holder, designed for magnetization measurements of powder samples at 4.2°K, appears to have eliminated the noise problem experienced with the previous sample holder. (c) The carbon resistance thermometer for the low temperature range is almost completed.

b. Experiments Using the Vibrating-Coil Magnetometer

An experimental program is under way to investigate the static properties of single-crystal ferrites before making window frames for a domain-wall study. It is hoped that in this way an internally consistent set of data can be obtained to provide a better understanding of the wall-relaxation phenomenon. Two disks of manganese ferrite, sliced in the (110) plane, are being used in this experiment. The magnetostriction of both samples has been measured as a function of temperature from −80°C to 25°C. The resultant data has been tabulated, but the calculation of the magnetostriction constants has not been completed. Measurement of the anisotropy constants as functions of temperature are now under way on the first of these samples. The results of these measurements, as well as others to be undertaken on these samples, should be available during the next quarter.

Preliminary measurements of saturation magnetization at liquid helium temperature were made for the system $Li_x^{+}Ni_{1-2x}^{++}Ni_x^{+++}O$ and for several other new materials.

6. Evaporated Magnetic Films

The two basic questions concerning the use of thin films as memory elements in a digital computer are (a) the speed of switching and (b) the current required for switching. The problem of speed received the initial attention and has been reported in the previous Quarterly Progress Report dated 15 December 1956. Work in this area has continued, and an attack has been started on the second basic problem: the reduction of the current required to switch a film. Work has also been initiated this quarter on the problem of uniformity and reproducibility of the films. This is another problem which arises when an attempt is made to make a large array of magnetic spots, such as is required in a practical memory.

a. Speed of Switching

(1) Theoretical: Numerical calculation from the theory has been made by means of Whirlwind I and has yielded specific predictions of sufficiently unique character to lend themselves to a rigorous experimental test. For example, a marked degree of overshoot of the magnetization before coming into equilibrium is predicted for certain values of switching field.

(2) Experimental: The switching apparatus required to study transient phenomena in the range, 1 to 10 mμs, has been under steady development and has been substantially improved in the last quarter. It is hoped that most of the problems have now been solved and that definite results will soon be forthcoming.

b. Current Required for Switching

Films depositied in a d-c magnetic field develop an axis of minimum energy in the direction of this field. If Θ is the angle between this axis and the magnetization (M), the angular energy dependence can be described by $E = K_u \sin^2 \Theta$, where K_u is a uniaxial anisotropy constant. The switching field is given by $H_s = 2k_u/M$; since the switching current (I_s) is proportional to H_s, we see that I_s is also proportional to K_u. Films deposited in a d-c field turn out to have an $H_s \sim 2$ oersteds; for a film diameter of 4 mm, a driving current of 400 ma is calculated. In order to drive films from high-speed transistors, this driving current must be reduced by at least one order of magnitude.

We can imagine that if it were possible to make an isotropic film, subsequent annealing in a d-c field should result in the development of a K_u which could be controlled in magnitude by controlling the time and temperature of annealing. It is natural to ask if deposition in zero d-c field would result in an isotropic film. Such would be the case, if the energy of atomic ordering processes responsible for K_u, were contributed by the external field. That this is not likely is immediately seen by noting that the internal magnetic fields responsible for ferromagnetism are of the order of 10^6 oersteds and that this field can also be expected to contribute to the uniaxial magnetic ordering process. Under these assumptions, the role of the external field is seen to be that of merely fixing the direction of the magnetic axis, not that of influencing the magnitude of the uniaxial anisotropy which is developed. Subsequent experiments in zero field have shown this to be the case.

It is now clear that deposition in a rotating field should make $K_u = 0$, since the internal field now will have no unique direction. Furthermore, deviations from a circular external field (elliptical field), as will be the usual case in practice, will not introduce a preferred direction along the major elliptic axis. Experiments in a rotating field of 25 oersteds have produced films in which $K_u = 0$.

However, it is found that even with $K_u = 0$, the films are not isotropic, but exhibit a fourfold symmetry, which is most naturally explained by assuming some degree of long-range crystallographic order. The complete energy expression now becomes $E_k = K_u \sin^2 \Theta + K_c \sin^2 2\Theta$, where K_c stands for a cubic crystalline anisotropy constant. For the particular case investigated, $K_u = (4/3) K_c$.

In the preceding studies it has been found convenient to work with films 200 Å thick in order to eliminate wall switching and simplify interpretation of the switching characteristics. Rotational

switching can now be studied by the low-frequency loop tracer described previously. The magnetic anisotropy of such films is studied simply by rotating the film in this loop tracer.

The next problem is to eliminate the fourfold axis, i.e., make $K_c = 0$. K_c is composed of two components $K_c = K_{xtal} + C\lambda^2$, where K_{xtal} is the contribution from crystalline symmetry, C is an elastic constant, and λ is the magnetostriction constant. For a free crystal $\lambda = \delta\ell/\ell$, the fractional extension during magnetization: for a clamped crystal $\delta\ell = 0$. Since the film is very thin and one side is fixed to the glass, it may behave as a clamped crystal with $\lambda = 0$. If this is true, K_c reduces to K_{xtal} and it remains only to make $K_{xtal} = 0$. For Permalloys in the range 65 to 75 per cent Ni, K_{xtal} is positive for a quenched alloy, and negative when slowly cooled. The proper intermediate cooling should lead to $K_{xtal} = 0$. Experiments are planned for the next quarter with this as the objective.

c. Reproducibility

There is considerable variability in the magnetic properties of films made in different runs or even in the same run. This is a serious problem, both in understanding the physics and in the engineering use of films. One approach to a solution of this problem will be in the direction of more and more refinement in the vacuum technique, the cleaning procedures for the substrate, degassing of the alloy charge, and general fabrication techniques. A spectrophotometer has been set up for chemical analysis of the films. In order to make these analyses, it was first necessary to determine the amount of iron present in various kinds of water. The results are given below:

Description of Sample	Quantity of Iron γ/ml
Tap water	0.43
First distillation in tin still	0.13
Second distillation in glass still	0.09
Third distillation in glass still	0.05
Triply distilled water exposed to air for 8 hours	0.29

$1\gamma = 10^{-6}$ grams

It can be seen from the table that in order to measure the iron content of the Ni-Fe films, the sensitivity will be limited by the care with which iron is removed and kept out of the water which is used.

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C. TRANSISTORS

1. Life Tests

The life tests that have been reported in previous quarterly reports have been terminated and the transistors have been unsoldered from the circuits for complete retesting. The results of these tests will determine whether or not it is desirable to reactivate the life tests.

Meanwhile, transistors are being life-tested in operating systems, e.g., TM-1, the multiplier; EMAR, the experimental memory address register; and the TX-0 computer. Selected transistors from these systems will also be completely retested and the results reported in the next quarter.

One hundred L-5122 surface-barrier transistors were removed from TX-0 after 1575 hours of operation and retested with the following results:

Median values	initial	present
β (3 v, 1 ma)	28	26
V_p, punch-through	9.2 v	8.9 v
$V_{ce\ sat}$ (8 ma, 2.5 ma)	70	72.5
$V_{ce\ sat}$ (2 ma, 0.3 ma)	48	50
I_{co}	0.9 μa	1.2 μa
I_{eo}	0.6 μa	0.7 μa
τ_B	49 mμsec	54.5 mμsec

2. Switching Transistors

a. L-5122

The L-5122 SBT, specified for switching applications, is now available from two sources, Philco and Sprague. Final work on the specification should provide tests to measure frequency ($h_{FE} \times f$); hole storage (K_s); and a saturation β. Complete data on the parameters of this transistor are presented in memorandum 6M-4955, "Parameter Distributions for the Philco L-5122 Surface-Barrier Transistor."

b. L-5134

The L-5134 MAT (microalloy transistor) has been delivered by Philco in two groups of 50 units each. Median parameter values for L-5134 MAT are as follows:

	1st 50	2nd 50
β at 1 ma, 3 v	145	215
β at 50 ma, 2 v	90	200
$I_{c\ sat}$ at 150 mv for I_b = 0.5 ma	24.7 ma	33.3 ma
inverse β at 1 ma, 3 v	12.5	11.5
K_s'	91 mμsec	105 mμsec
τ_s	71.5 mμsec	81 mμsec
I_{co} at 5 v	0.37 μa	1.1 μa
I_{eo} at 5 v	0.25 μa	0.76 μa
V_p	9.5 v	14 v

$h_{FE_N} \times 10$	50 mc/s	51 mc/s
$h_{FE_I} \times 5$	25.5 mc/s	16.5 mc/s
C_o at 3 v	3.0 μμf	2.9 μμf
τ_b, effective base lifetime	2.2 μsec	2.0 μsec

This transistor appears to be an extremely promising device and will solve a number of difficult driving problems in TX-2.

3 Transistor Switching Theory

In connection with a thesis at M.I.T., Johnston* has solved, by Laplace transforms, the partial differential equation for hole density in the base of a one-dimensional transistor. A transfer function is then obtained for common-base, common-emitter, and saturation operation. The common-base expression is

$$I_c(s) = I_e(s) \frac{\gamma_N}{\text{Cosh} \sqrt{\frac{W^2}{D_p} s + \frac{W^2}{L_p^2}}}$$

These transfer functions are then inverted into time functions by the conventional method and expressions are obtained which may, with a few approximations, be put into the form of the expressions of Ebers and Moll.**

A qualitative picture of the switching process in junction transistors is given in 6M-4870, "On the Behavior of Junction Transistors in Switching Circuits," by C.T. Kirk, dated 17 January 1957.

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Patricia Fergus
C.T. Kirk
R.C. Johnston

D. MEMORY

1. 256^2 Memory

All 38-digit planes were operating by mid-January and margins were taken in two parts using odd- and even-digit planes in tests using the 19-digit TX-0. Cycle time was 6.5 μsecs. Power supplies and power control have been giving trouble and an investigation of the power supplies has been started.

Members of Group 63 consulted with IBM at Kingston on the IBM version of the 256^2 memory. There seems to be no disagreement at this time and Group 63 will keep in close contact so that any difficulties encountered at Lincoln may be taken care of in the IBM design.

---

*Johnston, R.C., "Transient Response of Junction Transistors – I," M.I.T. Lincoln Laboratory Report 6M-4913 (21 February 1957).

**Moll, J.L., and Ebers, J.J., "Large-Signal Behavior of Junction Transistors," Proc.IRE, Vol.42, No.12 (December 1954) pp.1761-72.

2. Index Memory for TX-2

The index memory, designed to store index registers and program counters for TX-2, is in test operation. Access time is 0.6 μsec instead of the anticipated 0.8 μsec.

3. Transistor-Driven Core Memory (TDCM) for TX-2

Equipment needed for construction of the two 64 × 64 × 38 memory stacks for the TDCM has been delayed. A prototype model of a special core-positioning jig for the 50/30 mil cores needs more work; some apparatus for wiring one of the stacks in one piece has not arrived from the vendor.

Meanwhile, a new circuit has been designed for the read/write generator which should improve operation during the steady-state portion of the current, since the impedance will be increased from the previous level of 75 ohms to a new level of 500 ohms. The increased impedance will make the ONE signal received from the sense winding relatively independent of the number of ONE's in a word.

4. Thin-Film Memory

A model of a 4-word, 2-digit, thin-film memory has been constructed which operates with a cycle time of 0.45 μsec. Duty-cycle limitations of the peripheral electronics make high-speed operation obtainable only in bursts, but the model clearly illustrates the high-speed potential of this type of element for use in large memory-storage systems.

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E. DISPLAY

1. XD-1 Displays

A curvature of supposedly straight vectors on the XD-1 displays has been attributed to switching noise on the magnetic-deflection data lines coming from the frames. The vectors are straight when this noise is filtered out by appropriate level-setters. Any smearing of the E-characters, that remains after compensation of the magnetic deflection system, is also eliminated. The level-setters were used merely to show that the switching noise is the cause of vector distortion.

Although the exact mechanism by which the switching noise causes the distortion has not been determined, it appears to be capacitive coupling. A method of eliminating the noise itself must be found, since very little can probably be done to decrease capacitive coupling within the decoder to make it insensitive to switching noise.

2. Remote Display System

The basic circuits for the magnetic deflection decoders for the remote displays have been designed and are being built on TX-2 plug-in chassis. Delivery of some of the transistors has been slow and testing has been hampered. The decoder will essentially be an 8-stage, current-weighted, push-pull decoder which directly drives a magnetic deflection yoke. Full-scale deflection in 500 μsecs is more than sufficient for the present system and is accomplished with 3 volts across the yoke.

Tests have indicated that rise times of about 5 μsecs will be feasible for electrostatic deflection. Three- and seven-stage, current-weighted, push-pull, transistor decoders will be used to drive grounded-grid tubes. Since the current through the tubes will be controlled by the decoder, the tubes merely act as voltage buffers to supply the large voltage swings required for electrostatic deflection.

Whether or not the remote display will require an intensity gate has not been determined. Normally, the beam would be deflected to a blank spot on a character matrix when the beam is to be off. However, it is possible that the beam may have to be blanked during transit to a new character position, and an intensification gate generator is being designed which will consist of a gated RF transistor oscillator with a magnetically coupled, high-voltage detector to generate the large voltage-intensity blank gate at the low CRT cathode potential.

The flip-flop for the remote display has been given a thorough check for reliability with component variation and is ready for production in the TX-2 package. Transistors with the highest I_{co}, lowest current gain, and maximum and minimum τ_s (storage time) have been selected from a group of 500 2N123's for testing the flip-flop and other circuits. It is somewhat disturbing to discover how large variations of these parameters can cause so little change in the voltage margins. The flip-flop uses two saturating 2N123's in a simple circuit operating between 0 and −10 v. The collector load returns to −30 v but a diode "catches" the voltage at −10 v. Four input terminals are provided; two for each side. They may be used for independent set-and-clear inputs or, when an input from both sides is driven from the same source, they may be used to provide one or two complementing inputs. The input requirement is a positive pulse, 0.7 ± 0.4 μsec long, and 2.5 ± 1.2 v in amplitude, biased at −0.7 ± 0.2 v. The input resistance, which is about 210 ohms for complementing and 270 ohms for set- and-clear operation, can be complemented up to an input of 250 kcps and will resolve two triggers occurring 2 μsec apart when lightly loaded. The maximum output current at either 0 or −10 v is ±2 ma. An additional load capacitance of 1000 μμf may be carried.

The remote-display test-signal generator is completed and ready to produce dipulse patterns for the remote display circuitry. During checking of the generator, it was found that turning on laboratory power would destroy at least one transistor, even though the quiescent voltages were within rating. It was assumed that voltage surges occur when the switch contacts close at slightly different instants. When protective measures were taken against possible voltage surges, the transistor failures ceased.

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F. TX-0 AND TX-2

In a series of papers presented at the Western Joint Computer Conference in February, the story of the development of TX-0 and TX-2 through December of 1956 was given. A reprint of these papers was published as 6M-4968 and is included as Appendix 63-A to this Quarterly Progress Report. The following major parts of the development program are covered:

(1) History and Objectives
(2) Functional Description

GROUP 63

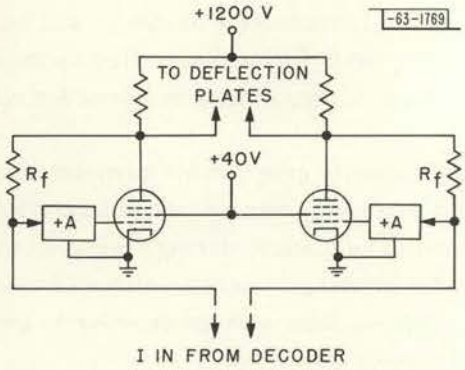

Fig. 63-1. Deflection amplifier.

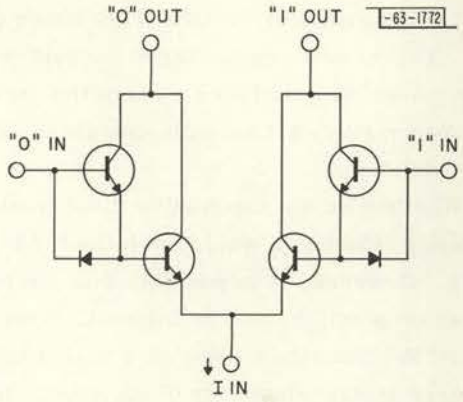

Fig. 63-4. Current switch.

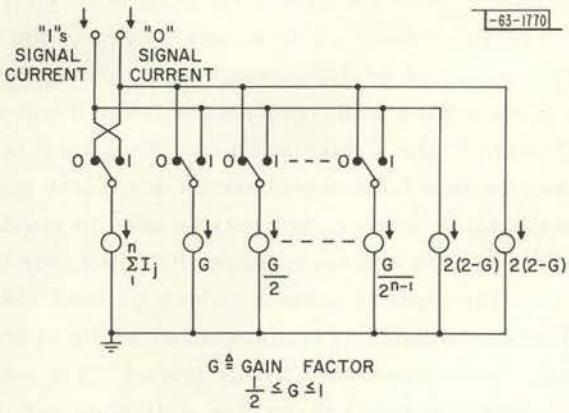

Fig. 63-2. Position decoder.

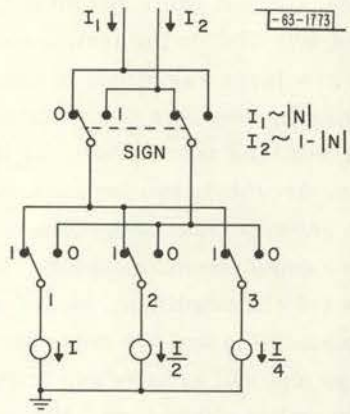

Fig. 63-5. Absolute-value decoder.

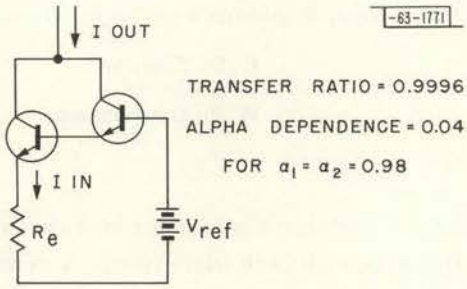

Fig. 63-3. Current source.

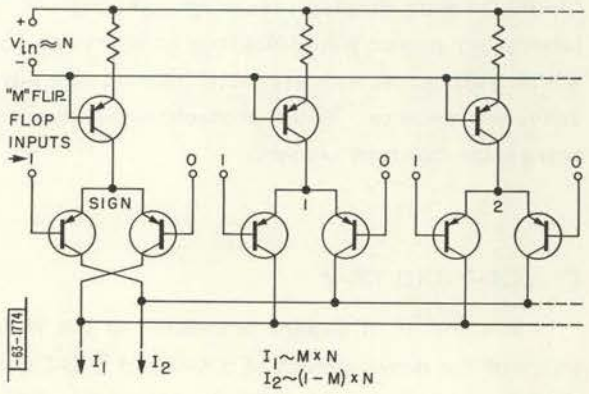

Fig. 63-6. Multiplying decoder.

TX-2 DISPLAY SYSTEM.

(3) Input-Output System
(4) Memory Systems
(5) Circuitry

Since the period covered by the conference papers, the following work has been done or is in process.

1. Display System

Two features are required of the display system for TX-2:

(a) a complete display every 12 μsecs, or less (two memory cycles),
(b) the sum of all errors due to nonlinearities, instability, etc., must be less than 0.1%.

A prototype display system has operated successfully with TX-0 for several months and has adequately demonstrated the advantages of using transistors in a fast, high-precision, electrostatic display system. The low operating voltages of transistors permit the cascading of decoders to generate nonlinear functions, compensating for cathode-ray tube aberrations. The deflection amplifiers, in which plate-to-grid feedback circuits are driven from high-impedance transistor sources, provide good matching of vacuum-tube and transistor characteristics.

The deflection system of the final design uses a 10-bit, push-pull, current-signal, transistor decoder whose outputs flow to plate-to-grid, feed-back amplifiers (Fig. 63-1), which have the following advantages over the simpler grounded-grid design: rapid response that is almost linear, with respect to time, to step-function current changes, and from which a current amplification can be obtained from input to amplifier output.

Figure 63-2 shows the general principles of the position decoder, each bit of which requires a switch in series with a current source that is adjusted to a negative power of 2, corresponding to its digit significance. (E.g., if the first-magnitude bit is adjusted to 1.0 ma, the second is adjusted to 0.5 ma, the fifth to 0.0625 ma, etc.) The two stages to the right have no switches. They prevent amplifier saturation and also help provide satisfactory gain control.

Figure 63-3 is a schematic diagram of the current source. The combination of two transistors acts as if it were one transistor with a β of about 2500. Stability is such that if each α changes by 1%, the output changes by only 0.04%. In a single transistor, the output, too, would change 1%. The output of the current source is the input to the current switch (Fig. 63-4). These two circuits use 2N167 transistors. In a typical lot, 2/3 of the transistors have $\beta > 50$ and $I_{co} < 0.6\,\mu a$.

Displays are improved if aberrations in the cathode-ray tube are corrected. In particular, dynamic focus correction greatly increases the total useful information displayed. To generate the required nonlinear functions of the deflection inputs, two special decoder circuits have been developed. The absolute-value decoder (Fig. 63-5) has a double-pole, double-throw switch activated by the sign bit. It recomplements the negative number, thus providing the same output for negative inputs as for positive inputs. The multiplying decoder (Fig. 63-6) forms the product of a digital number and an analog voltage, e.g., the output of a previous decoder. These correction circuits must use fast transistors and, thus, low-level signals, if corrections are to be set up

concurrently with the deflection amplifiers. Since transistors must be protected from destructive current surges when they are used in high-voltage systems, voltage swings of the decoder are limited by low-leakage, clamp diodes returned to ground by large capacitors with the shortest possible leads.

2. Power and Control

A new control for the present TX-0 and the new TX-2 power supplies has been designed and is being constructed. Power contactors in the d-c output lines of the power supplies have been eliminated, and the complexity of the timing and control networks has been reduced considerably. The a-c circuit breaker and contactor panel for this supply has been constructed.

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ESS SHAKEDOWN TESTING – WWI AND MTC OPERATION

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IV. ESS SHAKEDOWN TESTING – WWI AND MTC OPERATION
GROUP 64

A. SUMMARY

Thirty-two system shakedown tests have been carried out on the Experimental SAGE Sector covering the functions contained in Package A of the Direction Center Active (DCA) program during the three-month period since the start of system testing on 3 December 1956. System performance of all Package A functions, i. e., radar inputs, manual track detection and initiation, automatic tracking, data simulation, and recording, has been analyzed sufficiently to conclude that the system conforms to specifications for these functions in all major respects and that successful testing, to be started in March, can be expected with Package B of the DCA program.

To reduce the number of variables in gathering quantitative information for performance analysis, extensive use has been made of simulated and prerecorded radar data for inputs to the system. In addition, tests with live radar inputs, were carried out during February. Relatively minor defects in the program and in the equipment have been identified and are being corrected. It is expected that no serious problem will be found in the data still in the process of analysis.

The Memory Test Computer is regularly operating data-reduction and simulated-data-generation programs in support of ESS shakedown testing. Group 22 has also used this computer in SAGE simulation studies.

Most of the equipment modifications to WW I, required by the expansion of the Cape Cod direction center, have been completed and subsystem testing was started during the quarter. Subsystem testing of the input facility for AN/FST-2 data from South Truro was generally satisfactory.

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B. ESS SHAKEDOWN TESTING

1. General Plan

ESS shakedown testing of equipment, computer program, and operators as an integrated system started on 3 December 1956. Its purposes are diagnosis of system malfunctions and verification of the proper implementation of design specifications. Plans for this testing are built around the delivery dates for and the functions contained in the various packages of the direction center active (DCA) program.

The DCA program for ESS is being assembled in four packages. The functions contained in the packages and scheduled delivery times are as follows:

Package A was delivered on 3 December 1956. The functions include:

Radar Inputs
Manual Initiation
Automatic Tracking
Data Simulation
Recording

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TABLE I
TESTS PERFORMED WITH PACKAGE A

Test No.	Test Spec.	Input Data	Purpose of Test
1	6.1	Simulated (Ideal)	To provide opportunity for operator participation, test track detection and initiation, automatic tracking, ability of TBS personnel to use TBS facilities and acceptability of simulated data straight line paths.
2	6.1	Simulated (Normal)	
3	6.2	Ampex	To verify LRI conversion and transformation accuracy of DCA program, LRI, and Mark X radar compatibility with the DCA program, DCA program recording function. Test #3 used South Truro radar recordings. Test #4 used Bath radar recordings.
4	6.2	Ampex	
5	6.3	Ampex	To measure ability of automatic tracking programs to correlate, smooth and predict track positions using various combinations of input data parameters.
6	6.4	Live	To exercise and examine system operation using live radar data from long-range radar sites. First test of performance of radar inputs and radar mapping.
6A	6.4	Mixed	To back up test 6 if aircraft not available.
*S1	6.1A	Simulated (Ideal & Normal)	To extend operators' experience (similar to tests 1 and 2)
*S2	6.1B	Simulated (Normal)	To provide preview of system performance with overlap data from two long-range radars using simulated data inputs.
*S3	6.1B	Simulated (Normal)	To provide closely controlled inputs designed to measure the system's ability to smooth initial (upon initiation) track velocity errors.
*S4	6.1C	Simulated (Ideal)	To diagnose problems of and determine reliability of switch and light gun functions in the Training and Battle Simulation and Air Surveillance Rooms.

*S – Special Tests

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Package B is scheduled for delivery on 4 March 1957 and will include all the functions of Package A, plus the following:

Automatic Initiation
Track Monitoring
Height Finding
Manual Inputs
Identification

Packages C and D are scheduled for delivery on 3 June 1957 and will include all the functions of Packages A and B, plus the following:

Package C:

All Digital Displays

Package D:

Weapons Assignment
Intercept Direction
Antiaircraft Operations Center

Many of the test specifications required to define shakedown testing of the Experimental SAGE Sector have been prepared. Each test is designed to emphasize the operation of certain functions in the system, although data on operation of other functions will usually also be obtained. Each test called for by a given specification is generally performed more than once to provide sufficient data for analysis and is interleaved with tests for other specifications to allow a longer period for study and analysis of results.

2. Testing

a. Test Design

The general objectives of shakedown during the first three months were to:

(1) Provide quantitative data for analyzing system performance of the functions of Package A

(2) Detect malfunctions and deficiencies and to isolate their causes so that corrective action can be taken

(3) Present an opportunity for Air Force operators to gain experience in operating consoles

(4) Determine acceptability of simulated radar data for test operation

(5) Determine acceptability for test operation of radar data recorded on Ampex magnetic tape after transmission from remote radar sites

(6) Evaluate and improve test implementation, trouble reporting, and follow-up procedures.

Specifications were prepared for four special tests in addition to those for the six tests originally outlined in the General Test Plan. Two of the special tests were required to obtain further data for trouble diagnosis after initial tests had pointed out symptoms of trouble. The specifications covering testing during this period are listed in Table I.

Specifications covering the next three months of shakedown testing, using Package B of the DCA program, are listed in Table II. During preparation of specifications for a test of the track-monitoring function, problems were encountered in preparing the necessary simulated-data-input

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TABLE II
TESTS SCHEDULED WITH PACKAGE B

Test No.	Test Spec.	Input Data	Purpose of Test
7	6.5	Simulated	To emphasize examination of track monitoring, identification, and training of new operators. The examination will also include track detection and initiation, automatic tracking and TBS facilities using about 30 tracks in the system. First use of package B.
8	6.6	Ampex	To test overlap tracking which is important to this and all future tests. Similar to test # 7 but using recorded radar data inputs.
9	6.7	Live	To use live radar inputs in tests similar to tests #7 and #8. Radar mapping added.
11	6.9	Live	To examine the height-finder function using live radar data to check correlation of information between height-finder sites. Three height finders will be used separately and then together.
11A	6.9	Mixed	To back up test #11.
**12	6.10	Mixed	To examine radar inputs including gap-filler radars.
**12A	6.10	Mixed	To use aircraft participating in Cape Cod System Test. Otherwise same as test #12.
**13 **13A	6.10	Mixed	To repeat tests 12 and 12A with different flight paths.
*S5	6.10	Simulated (Ideal)	To test automatic tracking around turns under a wide variety of conditions.

*S – Special Test

**Tests numbered 12, 12A, 13, and 13A will be comprehensive tests of all air surveillance functions.

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TABLE III
SUMMARY OF TESTS PERFORMED
3 December 1956 – 28 February 1957

Test No.	Input Data	Number of Times Test Performed	
		3 December 1956 31 January 1957	February
1	Simulated	5	
2	Simulated	1	1
3	Ampex	5	
4	Ampex		1
5	Ampex		1
6	Live		(2)**
6A	Mixed		6
*S1	Simulated	4	
S2	Simulated	4	
S3	Simulated	3	
S4			1

*S – Special Tests
**Two tests scheduled – neither performed successfully.

tapes using the Memory Test Computer (MTC) program. These input tapes require many crossing-track and other complicated tracking situations.

The problems arose because it was found difficult to specify track parameters with sufficient accuracy to guarantee the crossing situations desired or to avoid MTC program halts resulting from programmed checks on heading errors. Expedient methods were devised to solve these problems so that the needed tapes could be prepared:

(7) Preliminary program runs were made in order to measure inaccuracies and determine values for corrections of the input parameters for the final program run.

(8) Improved plotting techniques were used to determine parameters more accurately.

(9) Hand calculations were used to determine critical parameter values.

Better long-term solutions to these problems are being developed.

b. Test Implementation

Thirty-two tests have been performed: ten in December, twelve in January, and ten in February. A breakdown of these tests is given in Table III and an accounting of computer time for system testing is given in Table IV.

Overlap tracking, using live input data from two long-range radars, South Truro and Bath, was tested on four occasions. No major difficulties were encountered. Preliminary analysis of the results of these tests is given in Section 3.b., 2 of this report.

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TABLE IV
SUMMARY
(Assigned Testing Time)

	System Time Summary			
	3 December 1956 30 January 1957		February	
	Minutes	% of Total	Minutes	% of Total
SYSTEM OPERATION	3394	66.8	1591	73.8
Equipment checkout*	37	0.7	54	2.5
Start-stop procedures*	127	2.5	166	7.7
Program trouble	70	1.4	0	0.0
Equipment trouble	1267	24.9	333	15.4
Miscellaneous lost time	186	3.7	14	0.6
Total time	5081	100.0	2158	100.0
Number of test periods	22		10	
	Equipment Failure Summary			
Interrupting failures	58		28	
Non-interrupting failures**	80		107	
Mean free time† (minutes)	65.8		65.1	

*Not tabulated separately for month of December 1956. Included in SYSTEM OPERATION totals for that month. (Equipment checkout not scheduled to be part of system time.)

**Not tabulated in December. Figure given is for month of January.

†Total time, less equipment trouble time, divided by interrupting failures.

Controlled live aircraft were scheduled for two test periods. The first test was unsuccessful because of a computer malfunction. However, an Ampex recording was made of the input data for use in future testing. The second test was cancelled because of aircraft unavailability. Additional tests with live aircraft are scheduled for March.

3. Test Results

a. Summary

The general objectives of shakedown testing for the first three-month period (see Sec. 2.a.) have been met. Considerable data is still in the process of analysis, which will lead to further information on system performance of the functions of Package A of the DCA program. However, sufficient information has been obtained to permit the conclusion that testing of program Package B should be initiated and that the residual analysis of Package A functions will not invalidate results with the new package. The malfunctions and deficiencies which are under study, or which have been isolated but not yet corrected, are either in areas that can be

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TABLE V

EQUIPMENT PROBLEMS – SUMMARY

A. Problems Resolved:

1. Repeated checksum errors, when reading from tape, were sharply reduced by improved maintenance on tape drives.
2. An automatic camera was installed at the LRI Monitor to satisfy a special recording requirement for data analysis.
3. Proper adjustment of the Raydist equipment permitted it to receive the required double timing pulses generated by the program.

B. Corrections in Process:

1. The telephone headsets being used by test personnel are uncomfortable and Bell Labs are cooperating in finding possible solutions.
2. Distorted displays, crooked vectors, fuzzy symbols, tails on radar data and vectors not originating from the character E were corrected by a temporary circuit change.
3. An investigation by NET&T of the busy condition of line selectors indicated the need for three additional line selectors. The traffic department is preparing a recommendation.
4. A joint IBM – Lincoln meeting to discuss adjustment criteria of display consoles resulted in a proposal to use a photoelectric calibration meter. IBM will evaluate the proposal by using this procedure for adjusting consoles scheduled for use during shakedown tests.
5. Three production light guns are being used as standards to determine proper adjustments for light guns being used in Building F.
6. Special springs have been ordered by IBM to correct pushbutton latching failures. In addition, IBM will test production-style pushbuttons in some of the consoles in shakedown.

C. Problems under Study:

1. Causes of activate button failures and intermittent light gun operation are not known but are believed to be associated. A diagnostic test, Specification 6.1C (special test #S4) has been designed to yield additional information to help analyses of these problems.
2. Drum LRI parity-checking circuits have been modified but the change is only a partial solution. Investigation will continue.

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avoided or are such that effects can be minimized by modification in test design. The facilities for using simulated data tapes and Ampex recordings of radar data as inputs during system tests of the direction center have proved to be acceptable, and the organization of test teams for conduct of tests and reporting of results has been satisfactory.

The following paragraphs describe specific results on various aspects of the system shakedown testing. Summaries of equipment problems and program problems are given in Tables V and VI, respectively.

b. Analysis of System Functions

(1) Radar Inputs

The analyses being conducted are: (a) that of the accuracy of the data conversion and transformation process in the DCA program and (b) that of the accuracy with which the system reports aircraft positions.

The data needed for the above analyses are not normally available through the recording features provided in the DCA program. Therefore, a means for using the special program-assembly-test recording to provide some of this data was devised and successfully used in seven tests. This recording provides radar coordinates (r, Θ) for selected frames of input radar data and corresponding system coordinates (x, y) resulting from the conversion and transformation process. True values for converted data are manually computed from the radar coordinates (r, Θ) for comparison with the values developed by the DCA program. Computations were made for 62 data points that were selected to give a distribution of r, Θ values in all quadrants about a radar site (South Truro) and to give x, y values in all quadrants of the ESS

TABLE VI

PROGRAM PROBLEMS – SUMMARY

A. Problems Resolved:

1. The DCA program was corrected to:
   a. Cause the hour digit of the real-time clock to advance.
   b. Permit use of changes in blip-scan with manually simulated data.
   c. Search the DCA tape to check data on Startover Mode 4 and make sure proper drums are cleared.
2. Changes to the display of the attention symbol forced on the initiator display by the Initiation Supervisor were added in Package B.
3. Sequence parameters in Package B were corrected to permit the Initiation Supervisor to force the attention symbol on the displays of Track Initiators #4 and #5.

B. Problems under Study:

1. A request that markers be properly written on the crosstell input drums by the startover program.
2. Changes in the DCA program have reduced the frequency of output teletype alarms which were caused by a timing problem. Investigation will continue.

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coordinate system. These computations showed that the mean positional error introduced by the conversion and transformation process in the DCA program was 0.044 nautical mile, and the standard deviation was 0.015 nautical mile. The maximum positional error, 0.100 nautical mile, was found at one point which had the largest radar range, 184 nautical miles. These data fall within the tolerances set by specifications for the radar-inputs function.

Additional data must be gathered from all areas using various radar sites throughout the sector before this study can be considered adequate, so that it is not expected that this study will be completed until data from several future tests has been collected and analyzed.

In order to measure the accuracy with which the system reports aircraft positions, it is planned to use Raydist recordings as the reference. Attempts have been made on two occasions during the month to record Raydist information on controlled aircraft without success because the Raydist equipment did not properly synchronize with computer-generated timing pulses on one mission and Raydist-equipped aircraft were not available on the second mission.

The Raydist equipment difficulty has been identified and corrected but there is a problem in the acute shortage of Raydist-equipped aircraft.

(2) Track Detection and Initiation

Experience obtained with live radar inputs, in addition to the experience with simulated and recorded tests, has established that track initiators can satisfactorily initiate on simulated or recorded input data,or live data from either search or Mark X radars. The track initiator starts a track by inserting an estimated speed and heading. The system then uses radar data to refine the course and speed to an established track. The time interval is somewhat longer than desired and a study is being made, using simulated inputs, to determine in detail the system's tolerance to insertion errors and the parameters affecting the time interval. The tests were designed to use both manually controlled track data from the miscellaneous simulation generation (MSG) feature of the DCA program and tape recordings prepared with the simulated-data generation (SDG) program on the Memory Test Computer. Errors in the SDG program, which were not corrected until about 15 February (see Sec. 3. c), prevented testing with tape inputs as scheduled. In an attempt to gather some information on transient conditions using the MSG feature of the DCA program, it appeared that inherent quantization in the data simulation caused oscillations in the velocity components of the track so that analysis from this information is difficult and probably inaccurate. Further studies of this problem will be carried out in March using data generated by the SDG program and data recorded on Ampex tape.

(3) Automatic Tracking

The automatic tracking function of Package A has been extensively investigated during our shakedown testing. We have examined single-radar tracking under simulated, Ampex-recorded, and live input conditions. Failures to meet program specifications have been corrected. The life of tracks, carried without aid from track monitoring and with single-radar coverage from South Truro, averages twenty minutes which is equivalent to an average track length of 140 nautical miles for an aircraft speed of 425 knots.

Data from two overlapped long-range radars was used on four occasions to get preliminary information on overlap tracking prior to the scheduled March tests. Immediate analysis was not possible because the necessary data-reduction programs were not scheduled to be available until March. Because Package A of the DCA program does not contain an aircraft altitude correction feature, reasonable accuracy in overlap tracking can be expected only in restricted areas where errors due to lack of slant-range correction are at a minimum.

However, the testing provided the following information:

(a) The orientation and calibration of the radars is sufficiently accurate for the program to accept data from both Bath and South Truro for tracking purposes.

(b) Data from a few samples suggests that there was insufficient system accuracy to permit data from both sites to fall consistently within the small search area. In most of these samples, the program frequently appeared to shift the small search area so that it sometimes enclosed the Bath data and sometimes the South Truro data. Tracking under these conditions is equivalent to using one radar during any given frame. During one 15-minute sample, however, when an ESS-controlled aircraft was flying at a range and altitude where lack of height corrections was insignificant, data from both radars appeared to be falling within the small search area. Further reduction and analysis of this data are in progress.

(c) A few tracks occurred where it could be observed that data from the Bath radar enabled the system to maintain tracking through a large clutter area that was mapped out at South Truro.

There have been two instances where the details of automatic tracking point to either minor difficulties in the operation of the DCA tracking program or to deficiencies in the test and analysis procedures. Both instances are associated with system performance during tracking around turns. These were investigated by:

(d) Theoretical analysis of variations in track speed which result during a turn at a given angle of bank (constant acceleration), and comparison of observed track-speed variations with predicted values.

(e) Observation of tracking performance for both right and left turns having different turn angles and different track speeds.

Investigation of (d) above, by plotting turns of two live tracks and four simulated tracks, revealed that observed variations did not agree with predicted variations. From theoretical considerations, it was expected that track speed as computed in the DCA program would decrease as a track executes a turn. The results obtained from the small sample of six tracks, however, showed speed increases during turns. Further analysis is needed to explain the differences observed. The theoretical calculations of speed variations must be reexamined and a larger sample of experimental results obtained.

Investigation of (e) above, by analyzing 48 turns in terms of track merit using manually simulated input data, indicated that the system tracked somewhat better around left turns than around right turns. The study of the MSG program which has uncovered peculiarities in data for turns due to quantization suggests that the analysis of the 48 simulated turns may not be significant. Further analyses will be made using inputs generated by the SDG program.

Group 67 discovered a DCA program error which would degrade tracking around turns in either direction. It is not apparent that the error would generate dissimilarity between right

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and left turns. The error has been corrected in Package B of the DCA program to be delivered in March.

(4) Data Simulation

Peculiar behavior of data has been observed while using the MSG program during analysis of track detection and automatic tracking. Track speed and heading and turn performance are affected by this unexpected system action. The MSG performance results from quantization or round-off in the quantities used in the program calculations. Some results obtained are:

(a) Magnitude of heading errors is a function of track speed, track heading, and the time interval between successive operations of the MSG program. These errors create discontinuities in heading in going from straight-line paths to turns. It appears that an error of several degrees can exist under certain conditions.

(b) Magnitude of speed errors is dependent on nominal track speed and the time interval between successive cycles of the MSG program. Errors of 10 per cent might result during typical use of the program.

(c) The effects of quantization also provided explanations for the following observed behavior:

1) Radius of turn appears to change during progress of turn.

2) A track sometimes appears as though it had remained too long in the turn maneuver and then turned back to correct its heading and compensate for the overshoot.

c. Support Programs on the Memory Test Computer

(1) Data Reduction

Priority effort has been placed on completion of additional MTC data-reduction programs to provide logs of station actions. In addition, existing histogram and scatter-plot-data-reduction programs are being arranged to provide plots of some of the basic outputs of analyses of automatic tracking quality (track life, trouble-free track life, etc.) System testing made it evident that the scope of these programs should be expanded beyond original plans. Necessary modifications have been worked out and it is expected that these programs which total about 6000 computer instructions, will be satisfactory for use by 8 March.

Other programs now being checked out will provide:

(a) Printout of data correlated with specified tracks to provide reduced data for analysis of overlap tracking.

(b) Printout of summary information about specified tracks at the time of and immediately following initiation.

(c) Printout of radar data coordinates (r, θ) as read from the radar-inputs drum and recorded by special use of the assembly test recording program to facilitate analysis of the radar-input data conversion and transformation process.

(2) Simulated-Data Generation

The MTC simulated-data generation (SDG) program was modified to correct inaccuracies which resulted in discontinuities at turns and to incorporate noise and blip-scan features. Tapes produced by the modified program have been successfully used for shakedown tests. Additional tapes are expected to be used extensively in March.

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4. Participation of Cape Cod Testing Personnel in the ESS Testing Effort

Groups 22 and 64 have initiated a joint effort in ESS system testing to realize the most benefit from experience gained by Group 22 in Cape Cod System (CCS) testing. Similar problems are involved in testing both systems, particularly in the conduct of tests, the reduction of recorded data, and the analysis of results.

The initial joint activity is primarily in the area of data-reduction programming. Computer programs prepared for reduction of CCS test data are being modified for use with data from ESS tests. A new data-reduction program is being designed to provide a more precise measure of the accuracy of position, speed, and heading computations made by the automatic tracking feature of the DCA program. Tests on the CCS have demonstrated the need for such a data-reduction program which, in addition, may reduce the amount of Raydist recording required for ESS tests.

The plans for the analyses of the various system functions are being studied jointly to select criteria for measurement of system performance consistent with those worked out for the Cape Cod System.

C. C. Grandy	Virginia Fitzpatrick	Jean C. Bryan
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J. C. Hodder	R. F. Russo	N. T. Jones
W. Ogden, Jr.	J. Slagle	E. Lafferty
J. J. Cahill, Jr.	D. J. Thomas	J. Monahan
A. Vanderburgh	M. D. Black	J. R. Nichols
Emy Brooks	R. D. Buzzard	P. Stylos
Carol Chomsky	D. R. Aufderheide	W. Woodward
Lois Earl	H. P. Bridge	H. F. Mercer

C. MEMORY TEST COMPUTER

The MTC system is operating data-reduction and simulated-data-generation programs in support of ESS shakedown testing. It is also used for SAGE simulation studies being conducted by Group 22. The importance of this support requires that improved reliability of MTC be continued as the major objective of this section.

The following investigations and improvements have been made during this quarter:

1. Marginal Checking System

Continued investigation of the marginal checking system uncovered more questionable circuits which were replaced. Decoupling of the selection-plane driver panels of the core memory was found to be very critical. As much as 40 volts ripple was found on the +150 volt supply line of some of the panels, when they were improperly decoupled. Incidence of spurious core parities, caused by noise on the +150 volt lines, was reduced when capacitors were installed across the supply lines. This modification reduced the ripple on the lines by a factor of about 5.

2. Drum Memory

Drum parity alarms occurring early in this period were eliminated by replacing some diodes and the cathode followers feeding the field selection matrix, and by adjusting the drum heads. A new drum-timing panel, with improved ground circuitry, was installed.

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There were no program interruptions because of drum parities during the last two weeks of February. Packaging for drum (timing channels) circuitry is being standardized for incorporation in the computer as permanent equipment. In the refined design, the photomultiplier was returned to +600 volts instead of +250 volts for a 60-fold increase of signal; a motor-driven variable autotransformer was installed to automatically erase the drum and initiate rewriting. The effects of temperature on drum operation were explored; it was found that the head gap decreases 0.0003" when the drum heats from 70° to 95°.

A head, with standard adjustment, can be run almost in contact with the drum but no damage can be done if contact does occur, since contact is made so slowly that the head is burnished by the high spots on the drum. However, it was found that even with the cover on, the temperature could be kept below 90° by maintaining correct tension on the belt and by blowing air over the motor.

3. Automatic Display Camera

The frequency with which the automatic display camera can be indexed is affected by the interval required to illuminate the data chamber each time the camera is indexed. The data chamber provides a means for identifying the scope pictures by serial number, date, time, or other special markings. An incandescent lamp normally provides illumination for the data chamber.

Gas-filled electronic flash tubes are being investigated as a possible improved light source. Two advantages might be realized:

(a) A reduction of index time from 475 milliseconds to about 350 milliseconds;

(b) An assurance of enough illumination in the data chamber to expose slower films that might sometimes be useful.

A two-flash-bulb system of illuminating the data-recording chamber was tried late in February with excellent results.

4. Tester for Plug-in Units

A plug-in unit tester was constructed that has one socket with all MTC voltages and signals and that incorporates a provision for diode and marginal checking. Adaptor plugs are used for the various types of plug-in units. The possibility of standardizing signal requirements to further facilitate testing is being investigated. The tester was successfully testing flip-flops by the end of this period, and experiments in testing gate-tube and buffer amplifier circuits were in progress.

5. TV Input System

Investigation of a special input system, using a TV camera as the pickup, is continuing. The camera scans printed copy and by means of special circuitry converts the copy to binary information to be fed directly into the computer. Circuits for quantizing video signals were redesigned and testing with associated circuits was started.

It is evident that the noise level will impose limitations on the size and complexity of the characters which can be resolved into digital data. System testing will start after completion and checkout of the quantizer for the TV input system.

GROUP 64

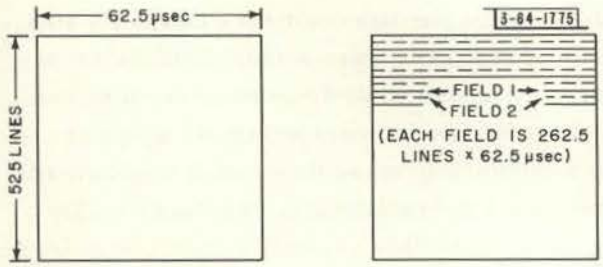


Fig. 64-1. Frame and two interlaced fields.

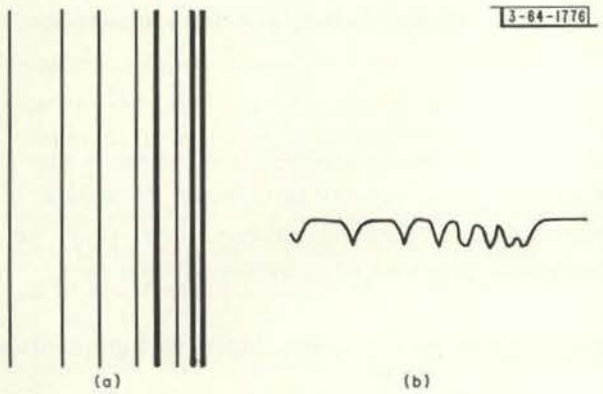


Fig. 64-2. Test pattern (a) and scope trace (b) of blank and unblank circuitry.

Fig. 64-3. Scope trace of a video input signal.

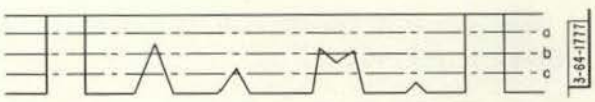
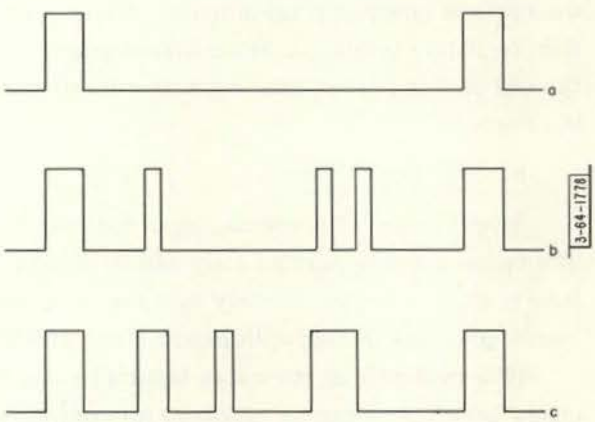


Fig. 64-4. Outputs received at various clamp levels (Ref. Fig. 64-3).



The prototype quantizer circuit for the TV input system is being built (see Quarterly Progress Report, 15 December 1956). It has been designed to operate essentially as follows:

One frame consists of 525 video lines by 62.5 μsec. Each frame consists of two interlaced fields, 262.5 lines by 62.5 μsec (see Fig. 64-1). Blanking pulses are provided at the end of each horizontal scan and at the end of each field to cut off the scanning beam so that it might return for the scan of the next line or field, leaving no trace during the return (or "flyback" time). Horizontal blanking pulses are 8.5 to 10 μsec wide, vertical pulses are 850 to 1000 μsec. Special circuits have been designed to generate "blank" and "unblank" pulses from the leading and trailing edges of the blanking pulses, respectively. These are standard MTC, 0.1-μsec pulses. Horizontal blank pulses clear the horizontal count to 0; horizontal unblank pulses index the vertical count and start the horizontal count of the next line. Vertical blank and unblank pulses clear both the vertical and horizontal counts to 0 at the end of each field and make all the necessary resets. It is expected that these blanking times will be used for some data processing.

Figure 64-2 represents the test pattern used and the scope trace that resulted in tests of this special blank and unblank circuitry.

A transistor video amplifier and clip circuit has been designed and a prototype built which will, in part, compensate for the varying amplitude of the trace of scanned material which results from the rise and fall times of video pulses. Figure 64-3 represents a scope trace of a typical video input signal.

The width of the pulses, or the spaces between them is governed by the width of the lines or spaces in the visual material being read. Outputs that result from varying a clamp level are indicated by (a), (b), and (c) of Fig. 64-4. It will be noticed that some information is lost at each level. The clamp has been made variable from 2.0 to 7.3 volts, allowing signal selection for obtaining maximum usable information and minimum noise.

6. MTC Computer Operation

MTC operation and reliability for this quarter, measured over 2-week periods, are as follows:

Scheduled computer hours	1776.2
Interrupting incidents	208
Hours lost	234.3
Per cent good time	88.4
Mean time between failures (in hours)	7.4

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D. CAPE COD ENGINEERING

1. Cape Cod Expansion

WWI is being modified according to plans formulated by Group 22 to make the Cape Cod System (CCS) a more useful tool for experimentation and evaluation of air defense functions. Most of the equipment changes required were completed and subsystem testing started.

a. AN/FST-2 Input Facility

The equipment for processing incoming AN/FST-2 data from search and height-finder radar at South Truro was subsystem tested. One modified channel from Bath was also tested. The tests were generally successful. Minor difficulties with both WWI and AN/FST-2 equipment were found and corrected. Modification of the second Bath channel was not completed until late in February; pulse testing of this channel will start early in March.

b. Display System

Display system changes were completed and the quality of the displays has been improved. A marginal-checking display program was written to test the deflection circuits, the vector generator, and the numerical waveform generator.

c. Reduction of Block Transfer Time, Core and Drum Memory

The investigation to find a method for reduction of block transfer time between core memory and magnetic drums is continuing. Several proposals are being studied to find the best features of suggested synchronizer systems and to combine them in a straightforward logical manner with a minimum of equipment changes. One such combination requires the addition of one flip-flop and a gate tube to the drum synchronizer to:

(1) Permit adequate timing of the restoration process so that the computer block-transfer cycle will not be lengthened,

(2) Prepare, in advance, for possible succeeding initiations in a block,

(3) Clear itself if initiations fail to come on time because the computer is stopped or because the block transfer is completed.

d. Automatic Teletype

The automatic teletype output system from WWI to Hanscom was completely subsystem tested and in operation early in February. By the end of the month, similar facilities were installed at Otis, Weymouth (Naval Air Station) and Westover.

e. High-Speed Input-Output Equipment

Group 22 requested further investigation of available equipment to increase speed and flexibility of WWI inputs and outputs and to provide a high-speed means of communication with XD-1 and MTC to speed up data reduction and analysis and CCS tests. Orders were placed for a high-speed line printer which is expected to be delivered during the next quarter, and the necessary design changes at WWI are under way.

2. WWI Computer Operation

WWI operation and reliability for this quarter, measured over 2-week periods, are as follows:

Scheduled computer hours	1987.9
Interrupting incidents	80
Hours lost	34.7
Per cent good time	98.3
Mean time between failures (in hours)	27.9

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E. K. Gates, L. D. Healy, P. J. Murphy, A. J. Rowe

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VACUUM TUBES

GROUP 65

Youtz, P., Leader

Clough, T. F.
Palermo, J. S.
Tandy, P. C.
Twicken, S.

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V. VACUUM TUBES
GROUP 65

A. SUMMARY

Stromberg-Carlson produced 187 acceptable Charactrons at a production efficiency of 70.5 per cent. Machlett Laboratories qualified as second source of the Charactron and produced 31 acceptable tubes. The average life of Charactrons in the 74 display consoles of XD-1 and XD-2 was 5412 hours as of 28 February 1957. Thirteen of the sixteen Charactrons which were removed after an average life of 6130 hours failed because of low emission.

Production of Typotrons at Hughes Aircraft continued at a rate greater than the demand at IBM and Hazeltine. The 94 Typotrons in the display consoles had accumulated an average life of 6000 hours as of 28 February 1957. Eleven Typotrons were rejected from the consoles after an average of 4357 hours. After the display consoles in XD-1 were modified to increase the impedance of the A_3 voltage supply, no more Typotrons were rejected for gassiness. This modification was introduced in the production line at Hazeltine and retrofitted to all existing consoles. Hughes Aircraft, under contract to IBM, negotiated with Machlett to try to qualify as second source for Typotrons. Machlett Laboratories initiated their program on 24 January 1957. General Electric had the low-powered twin-triode (type 0528/6414) back into full production with a 50 per cent yield. The shrinkage was due to a spread of the plate characteristics and microphonics. A MIL (Military) specification for the 6414 is close to final agreement. Raytheon, the second source, has the tube under good control except for the problem of centering the plate-current characteristics.

Sylvania Electric had the dual-control gate-pentode (type 2420/SR-1782A/6888) back into production after a shut-down of several months because of a high inventory. All of the 6888 specifications have been established except for a minimum plate-current requirement at a 25-volt grid drive. Data is being gathered to set this limit. Bendix Aviation Corporation, the second source for this tube, has made minor changes in the design, but is achieving satisfactory overall quality.

Tung-Sol has continued its efforts to produce an improved 5998 without major design changes. Meanwhile, Bendix was given a study contract by IBM to determine the feasibility of reproducing the characteristics of the 5998 in a tube of considerably different design with a major increase in electrode spacing.

P. Youtz

B. DISPLAY

1. Charactron

Stromberg-Carlson cut back its production line again this quarter to 187 acceptable Charactrons due to the decreased demand at IBM and Hazeltine. Their production efficiency was 70.5 per cent, which was a decline from the 76.6 per cent of the previous quarter. Grid-emission and grid-cathode leakage were the prime offenders for rejection. At one point, there was an epidemic of rejects because of irregular gun apertures – a problem corrected by the vendor who supplied the guns.

GROUP 65

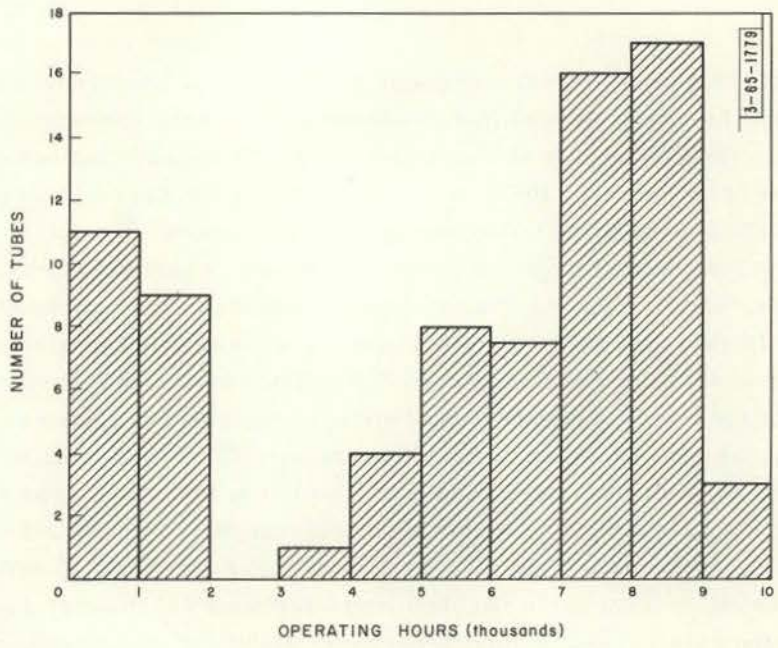

Fig.65-1. Distribution of Charactron operating hours in XD-1 consoles.

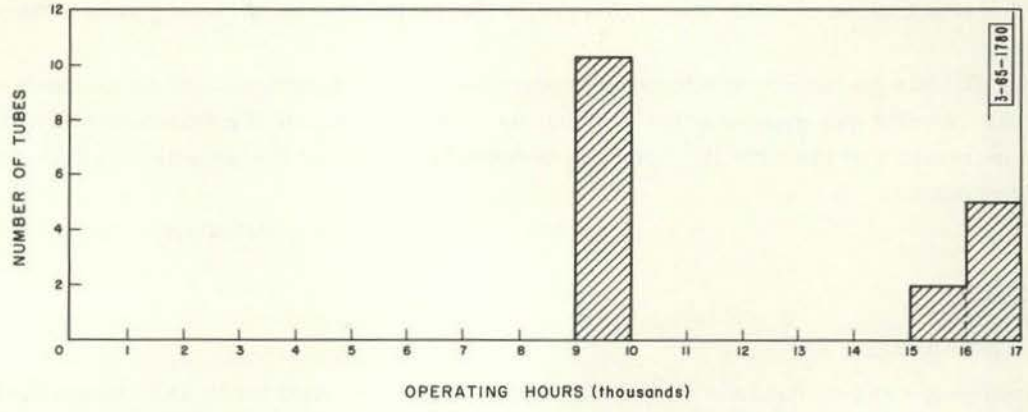

Fig.65-2. Distribution of Typotron operating hours on life test.

No tubes were rejected from the M.I.T. life racks this quarter. There are now ten 19-inch display tubes of which four have bariated-nickel cathodes on life-test. One tube with a bariated-nickel cathode has operated for 6385 hours and one with an oxide-coated cathode has operated 16,204 hours. Four early-production Stromberg-Carlson Charactrons were still operating after an average life of 9662 hours as of 28 February 1957.

The average life of Charactrons in the 74 display consoles was 5412 hours as of 28 February 1957 as compared to 5641 hours on 30 November 1956. The life history of these tubes as of 28 February is charted in Fig. 65-1.

Although ESS shakedown operations put a heavier demand on the situation display tubes, an average life of 6130 hours was recorded for the 16 Charactrons removed from XD-1 as compared to the previous quarter during which three tubes were removed after an average life of 4571 hours. As in previous quarters, cathode-emission was the factor which limited the life of the tube. Thirteen tubes failed because of low-emission, two were rejected because of poor focus, and one tube had a nonuniform cathode. The average life of the low-emission failures was 6597 hours. This would have been significantly lower if more current were used to get brighter displays. The phenomenon in which the tube focused to a line instead of a point and which appeared in 14 Charactrons in display consoles last quarter did not develop into a cause for rejecting tubes. This line-focus condition became progressively worse as the tube aged. All tubes exhibiting this phenomenon were rejected because of poor cathode emission. Stromberg-Carlson has so far been unable to isolate the cause. The same phenomenon was exhibited in an M.I.T. 19-inch display tube at its 10,000 hour life-point. At its 16,175 hour life-point, the tube was dissected. Although the suspected tabs on the first and second grid cylinder were removed and the cathode reprocessed, the tube continued to exhibit the same phenomenon. At this point the problem was turned over to the Stromberg-Carlson product improvement department. Last year Stromberg-Carlson contracted with Machlett Laboratories at Springdale, Connecticut, to set up a second source for the Charactron. Machlett is now producing the 19-inch situation display tube (Charactron) under the trade name of Scriptron. Since Machlett has no display-tube test equipment, Scriptrons were sent to Hazeltine for evaluation and acceptance. Of the 36 tubes sent to Hazeltine for evaluation this quarter, 31 were accepted by the Air Force. Production problems this quarter have been the helical-accelerator resistance and grid-cathode leakage. Both of these problems can be brought under control. Of the three Machlett tubes put on life test at Stromberg-Carlson during January, one tube developed a short and two tubes were operating satisfactorily at the end of February.

2. Typotron

Seventeen early-production Typotrons which have continued on the life-test racks of Group 65 were tested periodically to the IBM purchase acceptance specifications. Of the seven tubes which continued to meet all specifications, five have accumulated between 9001 and 10,000 hours while the other two have accumulated between 16,001 and 17,000 hours.

Since no end-of-life specifications have been established, Typotrons are kept on life test and in display consoles as long as they are operable without complaints from the operating personnel. A complete history of the 17 Typotrons on the M.I.T. life test, which have an average life of 12,286 hours, is charted in Fig. 65-2.

GROUP 65

Until this quarter, the only life-test positions available were at the Barta Building, M.I.T, Cambridge. Hazeltine has established four Typotron life-test positions at their Whitestone, Long Island plant and expects to have eight more available next quarter. There are no reports available on their life-test results.

Typotrons have been accumulating operational history in XD-1, XD-2, and the IBM test cells. No data were available from the McGuire site at the end of this quarter. The 94 Typotrons in the display consoles have accumulated an average life of 5999.5 hours as of 28 February 1957, as compared to 5276 hours as of 30 November 1956. The distribution of the life test hours is shown in Fig. 65-3.

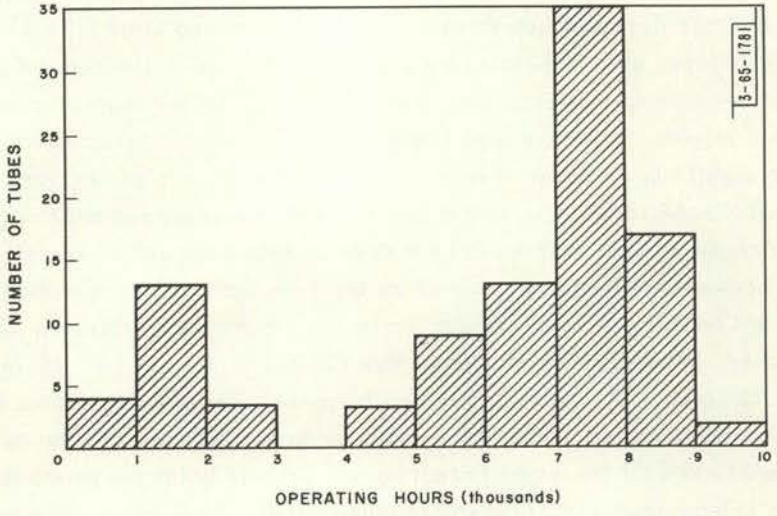

Fig. 65-3. Distribution of Typotron operating hours in XD-1, XD-2, and consoles being tested by IBM.

During this quarter 11 Typotrons were rejected from the display consoles with an average life of 4357 hours (see Table I), compared to 12 Typotrons rejected last quarter with an average life of 3558 hours.

It is significant that the number of Typotrons failures due to gas continues to decrease. This quarter these failures accounted for only 28 per cent of the total failures.

As a result of the failure analysis program held at the Barta Building and reported in the previous Quarterly Progress Report, the consoles in XD-1 were modified to increase the impedance of the A_3 voltage supply. All consoles in XD-1 were modified except the five which served as a test control. Also, Hughes Aircraft was asked to examine the design and processing of the tube to eliminate or at least to minimize the conditions which permit arcs to start within the tube and cause gassiness. The modification of the console increases the A_3 impedance which minimizes the sustaining of an arc which may start in the storage end of a tube. The effectiveness of this precaution is indicated by the fact that not a single gas failure has occurred in any modified console. Three of the gas failures for this quarter occurred before modification and the other occurred in a control console that was not modified. Also, no Typotron that has been installed

TABLE I
TYPOTRON FAILURE SUMMARY

Number of Tubes	Filament Hours	Stated Reason for Removal from Console
1	9	Flood-gun failed (gassy)
1	85	Gassy
1	1530	Poor storage
1	1639	Collector-mesh/storage-mesh short
1	4399	No flood-gun cutoff
1	5181	Gassy
1	6012	Gassy
1	6111	Poor writing-gun cathode
1	6655	Leakage between storage mesh and collector mesh
1	7343	Storage surface goes positive
1	8964	Low emission in writing gun

since the consoles were modified has failed for any reason. The tube dissection program to date has shown only a need for better welding techniques in the construction of the Typotron tubes.

C. RECEIVER TUBE RESEARCH AND ENGINEERING

1. Low-Power Twin Triode (Type 0528/6414)

a. General Electric Company

Early in this period, General Electric resumed full production which had been reduced in the late spring of 1956 to reflect lower demand by IBM and Burroughs. By the end of this quarter, the production yield was still below 50 per cent, due largely to a spread of the plate characteristics and microphonics. If G. E.'s efforts to improve production to a satisfactory yield are successful, inventories will soon exceed demand and the 1956 cycle of shutdown to deplete inventories and buildup to meet commitments will be repeated this year.

Final changes have been made to the 6414 MIL specification which is now in the hands of the military services. These last changes established the same life-test conditions for the zero-bias life-test that governs stability life-test. After six months' data has been collected, an addition will be made to the life-test end point to define the maximum change in plate current per tube over the life-test period.

b. Raytheon Manufacturing Company

Raytheon's progress as second source of the 0528 has been slow because of difficulties with grid-winding and plate-current characteristics. During the early stages of development, while special assembly facilities for the 0528 were being set up, they used grids from the commercial

grid department. Now that grid laths are set up for the 0528 in its own assembly area, the early problems of poor centering and nonuniformity should be corrected. Raytheon's major problem is that of centering the tube plate-current characteristics. If the zero-bias plate current meets design center limits, the plate current with −2 volts on the grid is too high. Raytheon and the joint IBM-M.I.T. tube groups are trying to solve this problem without introducing changes in the basic design of the tube.

2. Dual-Control Gate-Pentode (Type 2420/SR-1892A/6888)

a. Sylvania Electric Products, Inc.

Sylvania put this tube into production after a shutdown of several months to work off a ten-month inventory. The Brookville plant which is now responsible for all production of this tube type, has solved many of its early production problems and expects further improvements in quality.

All major points of the 6888 specification have been established except that for minimum plate current at 10-volt and 25-volt drives to meet AN/FSQ-7 system requirements. It is desirable that the pulse plate-current at the 25-volt drive also be set at the 130-ma level required for 10-volt drive. Test lots of tubes with the new geometry determined by Sylvania and M.I.T. have been made and are now undergoing extensive statistical analyses to arrive at reasonable manufacturing specifications.

The XD-1 failure rate for this tube (approximately 0.4 per cent per 1000 hours) has been higher than expected. Low plate current has been the important reason for removal. The problems of low plate current are being studied, as well as the high incidence of shorts and opens compared to the low power twin-triodes.

b. Bendix Aviation Corporation – Red Bank Division

Initial production reports from Bendix indicate their achievement of better plate-current centering and lower shrinkage with gold-plated molybdenum wire for the #1 grid. After extensive tests, they were given permission to use this wire rather than the gold-plated nickel wire used by Sylvania. Bendix has apparently learned to use the blackened wire used by Sylvania for the screen-grid and apparently concedes that a black surface may be necessary for dissipation purposes.

3. High-Power Twin Triode (5998/DT-438/2399)

a. Tung-Sol Electronics Corporation/Chatham Electronics

Production levels of the 5998 at Tung-Sol and at the second source, Chatham Electronics, have been so low that the tube was placed at the top of the IBM critical components list for duplex machines. A directive was issued assigning a definite portion of Tung-Sol's production to IBM. Tung-Sol's difficulties stemmed from tubes rejected for grid-emission. An extra radiator added to the bottom of the grid structure reduced the grid temperature and eliminated the problem. Some lots of tubes shipped to IBM by Chatham developed cathode peeling just beyond the 500-hour guarantee period. While Chatham and IBM have continued discussions as to the disposition of tube lots which exhibited this behavior, Chatham reported in January that

the cathode-peeling problem had been solved. As the quarter closed, current IBM requirements were being met, although production was insufficient to reduce the backlog.

Intitial specifications for a Tung-Sol version of an improved 5998 without major design modifications requires that the tube:

(1) meet IBM 2399 specifications, including M.I.T. shorts test and cutoff at −65 volts.

(2) operate at a heater power at least 20 per cent below that of the 5998

(3) use mica and metal snubbers rather than the present mica snubbers

(4) use one set of grid radiators at the top and another set at the bottom of the mount

(5) use plate structures which are not spot-welded.

Tung-Sol proposes to continue, with its own funds, an improvement program on the DT-438. An attempt will be made to open up the grid-cathode and the grid-plate structure by using a triode-connected tetrode with 5998 characteristics.

b. Bendix Aviation Corporation – Red Bank Division

IBM gave Bendix a study contract to determine the feasibility of reproducing the characteristics of the 5998 in a tube design with a major increase in electrode spacing. This became necessary after the DT-438 development had demonstrated that, exclusive of better manufacturing techniques, a really significant improvement in the reliability of the 5998 can be achieved only by an increase in electrode spacing, and possibly a complete redesign. Bendix proposed two approaches: (1) a twin-triode similar to the present one but with wider and longer cathodes; (2) four triode sections in one envelope with two pairs of triodes connected in parallel. The first approach was to use a modified 6080WB. In addition to the fact that this design requires an increase in the cathode area, initial results indicated that correct grid-pitch and dimensions had not been achieved. The second approach was to combine four triode sections in one bottle. At present, Bendix has an experimental triode called the TE-48 which has half the plate current and mutual conductance of the 5998. Preliminary tests on this tube type indicated that two sections might be combined to form each half of the present 5998 to produce a tube meeting specifications. Bendix was asked to run intermittent-shorts tests on the M.I.T. shorts checker using the TE-48 so that advance information might be gathered on the probable incidence of shorts to be expected with the design using the spacings of the TE-48.

4. Miscellaneous Receiver Tubes

a. Type 6072

Persistent difficulties in the Whirlwind I magnetic tape read-out circuits have been traced to a shift in the contact potential of the 6072. Because the operating point is too close to zero-bias, the normal shift of contact potential permits positive grid-current to flow through the large grid resistor. A high-current tube aggravates this condition which causes an important loss in gain for small negative-going grid signals. Redesign of the circuit at this time is not advisable because of impending equipment changes.

b. Type 5998 in TX-2 Core-Driving Circuits

Retest of a number of 5998 failures disclosed that cut-off characteristics had deteriorated seriously. This unusual condition was attributed to portions of the cathode that are free of grid control because of positional shifts of the grid during life. Only minor changes to be performed by the manufacturer are required to correct this fault.

c. Cathode Interface

The results of the ASTM interface round-robin tests, in which M.I.T. participated with the tube industry, will be punched on IBM cards for analysis by Bell Telephone Laboratories. Final designs have almost been reached for a standard triode, which will provide a better medium for such procedures as cathode-melt approval tests and permit better industry-wide comparisons of such data.

D. RESEARCH

1. Cathode Studies

Group 24 noted severe cathode poisoning in the cathode-ray tubes they were using for solid-state studies. During the investigation of the poisoning phenomenon it was necessary to devise certain tests to monitor the state of the cathode. Emission current from the cathode to any of the electrodes during activation and aging can be monitored for small changes. Any dip in current indicates a local or general poisoning of the cathode. This test reveals poisoning effects due to contamination from the electrode structure.

A partial poisoning of the center of the cathode would not be noticed in the current drawn to the grid, since the entire cathode contributes to this current. A second valuable test for cathodes in cathode-ray-tube guns is to monitor the beam current. Any small dips in beam current reveal the state of the center of the cathode. These two tests indicate whether the cathodes are poisoned by bombardment of the gun structure of the cathode-ray tube.

A space-charge test was devised on the assumption that the beam current from the average electron gun should be space-charge limited. A graph of beam current, as a function of heater voltage, should have approximately zero slope in the neighborhood of the normal operating point. Any marked deviation from the zero slope indicates a cathode with poor emission properties. This is a less selective test than the two previously mentioned and reveals cathodes which are unsatisfactory for any of several reasons other than poisoning.

The simplest way to carry out this type of test is to apply a fixed voltage to A_2, tie G_1 to cathode, and measure A_2 current as the heater voltage is varied. For a gun designed to operate at 6.3 volts, a suitable range of heater voltage would be from 5 to 8 volts. The slope of the resultant curve can then be used as a criterion for the state of health of the cathode.

This space-charge test has been used to monitor all cathode-study tubes and display tubes on life. It was also used in 25 experimental tubes that were built and evaluated to develop a method of processing an electron gun so that it could be put into a demountable system for electroluminescent studies. A chemical-cleaning and vacuum-firing process was developed to clean a gun thoroughly before its installation in a demountable tube.

2. Electroluminescent Layers

Thirteen tubes were designed and built for the electroluminescent studies of Group 24. Five of these tubes were used by Group 24 on their own vacuum systems to study electroluminescent layers under electron bombardment. Eight of the tubes were used by Group 65 to investigate:

(a) a surface whose photoconductive properties will not be destroyed by the high temperatures of vacuum-tube processing,

(b) a surface which will not contaminate the cathode by preventing its proper activation or by reducing its life to an impractical level.

Two techniques were developed to apply conductive coatings on electroluminescent plates; one method is to spray a film of stannic oxide, the other to evaporate an aluminum film.

SAGE DC AND CC SITES

GROUP 66

Morriss, B. E., Leader
McVicar, K. E., Associate Group Leader

Bragar, P.
Brock, L. T.
Callahan, T. R.
Croke, J.
Hedison, H.
Holden, W. E.
Ippolito, V.
Linehan, L. H.
Manning, F. F.
Mayer, R. P.
Roberts, A. J.
Sergio, L. S.
Shorey, R. R.
Shortell, A.
Smiley, E. L.
Thompson, S. L.

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VI. SAGE DC AND CC SITES
GROUP 66

A. SUMMARY

Group 66 is responsible for the adaptation, testing, and installation of the air defense computer programs at the first three SAGE sites. Because the RAND Corporation will perform this program installation for the Air Defense Command at subsequent sites, this group has been manned jointly by Lincoln and RAND. About 240 people were assigned to the activity as of 28 February 1957; the majority are RAND personnel recruited since RAND assumed this responsibility.

Group 66 activity is presently located at three places: Lexington, Massachusetts; Kingston, New York; and McGuire Air Force Base, New Jersey.

The Lexington activity consists of about 90 Lincoln and RAND staff members and is responsible for maintaining liaison with Group 67, Program Production; training new programmers in the operation of the air defense computer program (prior to 18 February); adapting the air defense computer program to the individual sectors in which it is to operate; planning the tests to be performed on the computer program at the sectors; and providing the necessary documentation services.

About 80 Lincoln and RAND staff members are located at Kingston and provide a field training station for utility and instrumentation program installation and a place for program installation teams to assemble before going into the field. The computers at Kingston also absorb some of the XD-1 overflow work for Group 67.

The air defense computer program is being installed in the AN/FSQ-7 at McGuire Air Force Base by about 70 Lincoln and RAND staff members. The McGuire Section also serves as an experimental model for future checkout teams and as a source of data for additional test planning.

The present schedule will require an estimated peak of approximately 550 people to install the computer programs throughout the SAGE System. This estimate has been based on a general review of the program installation to date. The review has been published as 6M-4911.

B.E. Morriss
K.E. McVicar

B. LEXINGTON

The computer program for the direction centers of the SAGE System has been written in such a way that one program, with modifications, can be used in all sectors. This program is referred to as the master DCA program and the parts of it which must be modified to fit individual sectors are the adaptation parameters. The values for the adaptation parameters required to fit the master program to the McGuire Sector are established by Group 67. Group 66, however, will be responsible for adapting the master program to subsequent sectors.

The complete computer program has been divided into four groups of subprograms (Packages A, B, C and D) that correspond to the functional buildup of the whole system of programs (see Section VII, B.1.). Package A of these subprograms was turned over to Group 66 by Group 67

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late in the previous quarter. The members of Group 66 in Lexington during this quarter checked, documented, and forwarded Package A to the members of Group 66 on site at McGuire for further checkout and installation on the AN/FSQ-7 there.

Group 66 has designed and conducted over the past six months a series of lecture courses for training new programming people in the installation of the computer programs at the sectors throughout the SAGE System. This responsibility was transferred from Group 66 to the RAND Technical Services Group on 18 February 1957.

Fifty-three people were transferred out of the Lexington training courses during the quarter as follows:

38 to test operations training at Lexington for subsequent transfer to McGuire and Stewart.

13 to Kingston to train in test facility and utility system operations for subsequent transfer to McGuire and Stewart.

1 to work in the adaptation section at Lexington.

1 to work in the documentation section at Lexington.

P. Bragar	L. Linehan
V. Ippolito	L. Sergio
R. P. Mayer	E. L. Smiley

C. KINGSTON

Training in utility program installation, computer operation, and test facilities continues at Kingston under the supervision of Group 66. About 1000 hours of computer time on the machines in the test areas and on XD-2 at Kingston have been available to and used by the Group 66 people there, providing them with valuable training before their assignment to a SAGE site. A better understanding of some of the practical aspects of program checkout has also been gained as a result of the cooperative relations that have been established with IBM computer engineers. Through the use of a mutual logging system, both the computer engineers and the program checkout engineers have contributed to the establishment of better tools for assessing machine reliability requirements.

The Kingston activity has also been a source of additional computer time for overflow work from XD-1 in the Experimental SAGE Sector, thereby helping to expedite the program checkout work there. Between three and four hours per day of computer time at Kingston was devoted to XD-1 overflow during this quarter.

A card room has been established in Kingston to provide the necessary punched card facilities for the site teams as well as a resource for the maintenance of the Group 66 master program file.

The Stewart program-installation team is presently assembling at Kingston in preparation for assignment to Stewart Air Force Base. The Stewart team is using the Kingston facility as an aid to training and for preparation of test plans and assembly test decks. By the end of this quarter, the Stewart team had completed about 20 per cent of their tests for the radar inputs function and had just started testing the tracking function. The computer programs being used

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in these tests are unadapted and the tests are being run primarily for training and test shake-down purposes.

K. E. McVicar
L. Brock
J. Croke
F. F. Manning

D. McGUIRE

Package A of the direction center computer program consists of some 30 subprograms which perform the basic air defense functions of radar inputs and tracking. These subprograms were adapted to the McGuire sector and checked out. Tests have been started on Package B which contains, in addition to those in Package A, the functions of height finding, automatic initiation, track monitoring, identification, and manual inputs.

A. J. Roberts
H. Hedison
R. R. Shorey
W. E. Holden
S. L. Thompson
T. R. Callahan
A. R. Shortell

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COMPUTER PROGRAM PRODUCTION

GROUP 67

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Zraket, C. A., Associate Group Leader
Benington, H. D., Associate Group Leader

Arden, Marguerite
Bagley, P. R.
Bailey, D. L.
Bensley, E. H.
Briscoe, H. W.
Budd, Eleanor
Burrows, J. H.
Byrne, W. J.
Carson, J. J.
Chandler, A. R.
Clapp, Elizabeth
Collins, L. B.
Ferguson, Mary E.
Fletcher, J.
Frachtman, H. E.
Gochman, H.
Hager, L. S.
Hazel, Inez
Hills, Merithew
Jones, K. L.
Kelley, Frances T.
Kirshner, H. J.
Latimer, D. P.
Lundberg, E. D.
Marko, J. T.
Marnie, G.
McEvoy, Eleanor J.
Miller, J.
Newhall, H., Jr.
Ornstein, S.
Patton, R. L.
Pendergraft, E.
Rising, H. K.
Roberts, T. A.
Rupp, A.
Shoolman, A. R.
Stone, Judith H.
Thomas, L. M.
Vance, P. R.
Wilson, L. D.

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VII. COMPUTER PROGRAM PRODUCTION
GROUP 67

A. SUMMARY

Operational specifications for a SAGE direction center have been reviewed with the 4620th Air Defense Wing. The computer program for the active computer of a SAGE direction center (the DCA program) was consequently improved and simplified, with a saving of about 35,000 registers of drum storage, and the excessive requirements for drum storage, which developed in the initial writing of the program, were eliminated. Adequate drum storage for the DCA program is thereby insured in AN/FSQ-7's, which have 102,000 registers, and the work load in assembly testing has been eased.

The version of the DCA program to be delivered to the McGuire sector on 1 June 1957 will require about 85,000 registers of drum storage (approximately 60,000 instructions, 25,000 tables) for all operational functions in the direction center except automatic crosstelling and forward-telling and duplex operation, all of which will require about 7,000 additional registers and will be ready for delivery by 1 September 1957.

The assembly testing and delivery of the DCA programs, covering a 100-track system, has been divided into four packages – A, B, C, D (see previous quarterly progress report). The operational areas and the programs comprising each package have been defined. Parameter testing, establishment of adaptation parameters for the Experimental SAGE Sector (ESS), and the design of the sequence parameters and the drum- and core-storage-allocation of all DCA subprograms, required for the June 1st program, were completed on 15 February 1957.

Assembly testing of Package A was completed and delivery was made one month ahead of schedules predicted in June-July 1956 – on 3 December 1956 to Group 64 for system shakedown tests on ESS. Package B was assembly tested and ready to be delivered to Group 64 at the end of the quarter. Package C was completed ahead of schedule and ready for delivery with Package B. Package D will be completely tested and released the first week of June. All packages are also being released to Group 66 along with the adaptation parameters required for installation on the AN/FSQ-7 at McGuire.

Methods for adapting the DCA program to individual SAGE sectors on a production basis have been designed and will be used during the next quarter.

J. A. Arnow
H. D. Benington
C. A. Zraket

B. DCA COMPUTER PROGRAM

1. Introduction

A review, by Group 67 and the 4620th Air Defense Wing, of original operational and mathematical specifications for a SAGE direction center disclosed opportunities for modifications and improvements which were subsequently documented in a set of memorandums listed in 6M-4902*.

*Collins, L.B., Durieux, C. (RAND), Wollin, B. (RAND), "A List of Memoranda Describing Recent Modifications of SAGE Direction Center Functions," M.I.T. Lincoln Laboratory Report 6M-4902 (6 February 1957).

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A saving of 35,000 registers of drum storage will be realized in the DCA master program from the modifications and from improved coding of some of the subprograms. The 1 June 1957 version of the DCA program, referred to as Package D, will require about 85,000 registers of drum storage for a 100-track system: 20,000 registers of tables that are required for storage of data; 8,000 registers of instrumentation programs and tables used in real-time testing of the system; 54,000 registers of program instructions; and 3,000 registers of drum-packing spares. Since the AN/FSQ-7 contains 102,000 registers of drum storage, the initial program is well within the capacity provided by the drums.

Package D will include all operational functions, except automatic crosstelling, forwardtelling, and safe-data-storage processing for duplex operation. These three functions will require about 7,000 additional drum registers and will be added to the system by September 1957. A list of the specifications which define the DCA program has been published as 6M-4082-11, "Initial Program Specifications List."

The DCA program was divided into four packages, A, B, C, and D. The operational areas are combined into the whole system of programs as follows: Each package includes all programs in previous packages plus those added for the functions indicated. A fifth Package E will add the functions of automatic crosstelling, forwardtelling, and safe-data-processing for duplex operation and is scheduled for delivery to Groups 64 and 66 in September 1957.

A Package	PO – Program Operation (Program timing and control, startover, instrumentation).
	RI – Radar Inputs
	TR – Tracking and Manual Initiation
	RC – Recording
	SM – Simulation
B Package	HT – Height Finding
	MO – Track Monitoring
	MI – Manual Inputs
	ID – Identification
	AT – Automatic Initiation
C Package	DD – Digital Displays and Command Post
D Package	MA – Telling to Manual AAOC's and Subsectors; Antiaircraft Direction
	WA – Weapons Assignment
	IN – Intercept Direction
	RF – Raid Forming

All necessary switch-interpretation, bookkeeping, and situation display subprograms are included for each operational area within the specified packages. Some 60,000 instructions (including those for instrumentation) make up the DCA program: about 24,000 are included in Package A; 15,000 are added in Package B; 6,000 in Package C, and 15,000 in Package D.

Parameter testing, establishment of adaptation parameters for the Experimental SAGE Sector (ESS), and design of the sequence parameters and the drum and dynamic core-storage

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allocation of all DCA subprograms, required for all of the above packages, were completed by 15 February 1957.

Assembly testing of Package A was completed and the package delivered on 3 December to Group 64 for system shakedown tests of ESS, and to Group 66 for installation in the AN/FSQ-7 at McGuire Air Force Base.

Assembly testing of Package B was completed at the end of the quarter and was ready for delivery to Group 64 on schedule. Package C was completed ahead of schedule and ready for delivery with Package B. These packages were also ready for delivery to Group 66, with the adaptation parameters necessary for testing at McGuire. Performance of Package A programs during shakedown tests has been very satisfactory; only a few minor errors have required correction.

Assembly testing of Package D will be started by 15 March. The package will be delivered in June to Groups 64 and 66. All program adaptation parameters required for the McGuire sector will also have been delivered to Group 66.

D. L. Bailey	Elizabeth Clapp	S. Ornstein
H. J. Kirshner	H. E. Frachtman	R. L. Patton
E. H. Bensley	L. S. Hager	E. Pendergraft
H. W. Briscoe	Inez Hazel	A. R. Shoolman
W. J. Byrne	D. P. Latimer	L. M. Thomas
A. R. Chandler	J. Miller	

2. Program Sequence and Storage Design

The storage and sequence parameters for the Package D programs have been designed with the primary objective of minimizing the transfer time of subprograms and data-storage tables between the high-speed magnetic-core memory and the input-output equipment (mostly drums). This reduction in transfer time, plus the overlapping of in- out and operating time whenever possible, will be reflected in a corresponding saving in program frame time. Another objective has been to minimize auxiliary- memory drum storage requirements in order to provide storage for the entire DCA program, including the subprograms to be added after 1 June.

Several techniques used in achieving the design objectives have been applied:

(a) The sequence in which subprograms operate has been arranged to permit sequential operation of subprograms having similar environments (i. e., data-storage tables and subroutines), except when program and operational design requirements prohibit.

(b) Data-storage tables and subroutines most frequently used together have been located contiguously on the drums and in core memory, wherever possible, so that the environment of a subprogram may be transferred with a minimum number of drum accesses.

(c) The transfers between the drums and core memory, normally required for small tables, have been eliminated by allocating permanent storage for the tables in core memory.

(d) Subprograms and tables have been packed more tightly on the drums in order to minimize the number of drum fields required for storage.

(e) Instrumentation programs, which operate in real-time during testing as part of the DCA program, have been allocated permanent drum storage. Other instrumentation programs time-share drum storage with certain DCA tables.

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It should be noted that the above changes do not affect the operational transfer function of the DCA system because they are accomplished by modifications to the program structure.

3. Adaptation

Geography, equipment, and facilities vary from one sector to another and the values for them must be inserted into each DCA program according to the sector in which the program is to operate. The method initially used to adapt the DCA program to McGuire and ESS required considerable knowledge of the SAGE System in general and of the DCA program in particular. In many cases, where similar information was required for many subprograms, the method was redundant. Therefore, a study was undertaken to specify a system that

(a) would be concise,

(b) could be used without a detailed knowledge of the DCA program,

(c) could be readily modified as required by equipment, program, or operational changes, and

(d) would provide efficient forms for recording all data gathered for, or generated during, the adaptation process.

The programs in Package B were adapted to ESS and McGuire using the initial method. An improved system as indicated by Fig. 67-1 and described as follows, is being used for adapting Package D and will be used for all subsequent adaptation.

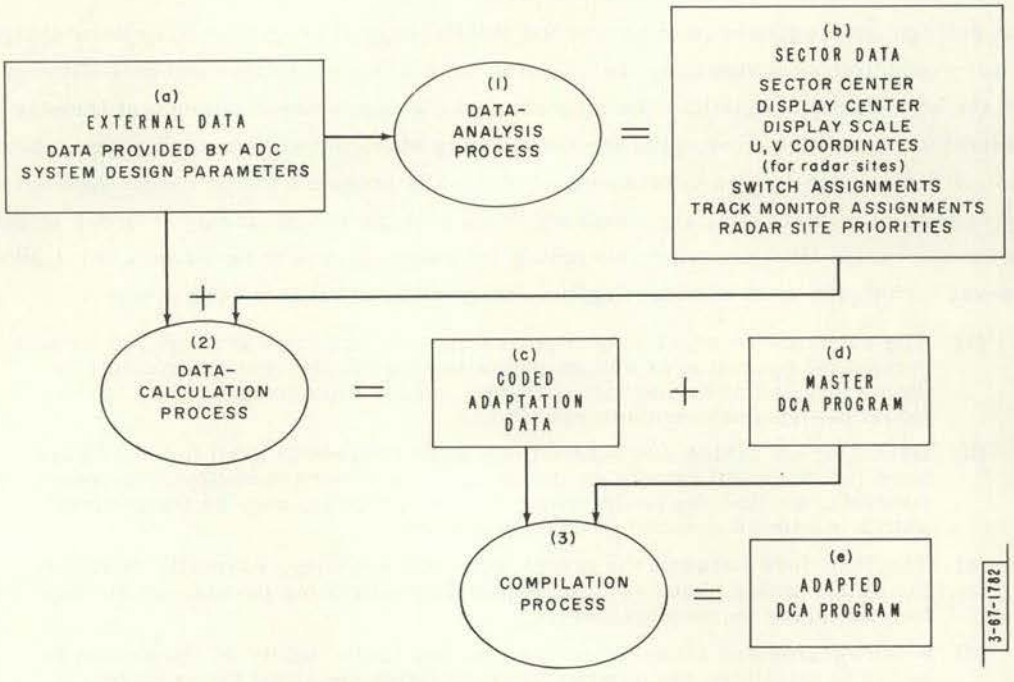

Fig. 67-1. Process for adapting the DCA program to individual sectors in which it is to operate.

Information supplied by the Air Force (latitude and longitude or radar sites and air bases, sector boundaries, etc.) is combined with certain system design parameters to form a block of information termed external data (a).

Step (1):– The external data is analyzed to obtain additional input data, termed sector data (b), that is basic to the adaptation process.

All items included in both external and sector data are tagged for ready reference.

Step (2):– External and sector data are fed through a data calculation process which also includes instructions for coding for specific programs or classes of programs.

Step (3):– The coded adaptation data (c) is compiled with the unadapted DCA program (d) to produce the adapted version (e).

It is hoped that the above process can essentially be written in the form of a computer program, thereby making adaptation almost fully automatic. Package B was adapted to ESS and McGuire and Package D to ESS during this quarter. All external data has been collected for the McGuire and Stewart Sectors. Actual adaptation of the DCA program to SAGE sites has been turned over to Group 66 who will use the methods developed by Group 67.

J. J. Carson

4. Frame-Time Study

A small group has been studying the problem of frame time – the basic period required to cycle through all the component parts of the DCA program. The immediate goal of this activity is to ascertain that the frame time of Package D will be within the operating requirements. The timing facilities of the control program, PEC (Program Environment Control), have been used to obtain rough measurements of operating time of the component programs of Package B. This information, together with estimates of operating times for programs added in Package D, will be used to estimate the frame time of Package D. The second goal is to develop a fuller understanding of the factors affecting program timing. To this end, more sophisticated timing measurements must be developed, as well as a broad spectrum of program-operating time and in-out transfer time models. These models and their analysis will eventually lead to the design of more efficient, hence faster, program operation. Results of this study will be reported in the next quarterly.

L. B. Collins

C. UTILITY SYSTEM

The Lincoln Utility System was evaluated and will be modified, primarily to conserve computer time, but also to provide means for the programmer to manipulate the system at the console, to increase flexibility, provide for more convenient detection and analysis of errors, improve the programmer's ability to compensate for errors, and to lessen the redundancy of both programming effort and storage requirements of the system.

Procedures were established for maintaining the documenting utility programs so that all users will be kept up to date. Nearly all desired documentation has been provided for the programs in the utility system, i.e., program specifications, flow diagrams, listing and tag table, operating directions, test specifications, and test deck.

P. R. Vance
P. Bagley
Marguerite Arden
L. Wilson
Judith Stone
Eleanor Budd

D. COMPUTER OPERATIONS OFFICE

XD-1 computer hours, assigned to Group 67 over the past quarter was used as follows:

	Lost Because of Equipment Failure	Turned over to IBM for Maintenance	Useful Time
DCA Assembly Test	31.49	75.23	411.87
DCA Parameter Test	23.64	15.20	140.02
Error Analysis and Overhead	5.30	17.99	79.40
Utility System and Input-Output Instrumentation	15.18	18.44	203.88
Total	75.61	126.86	835.17

Total Assigned Time: 1037.64 hours.

J. H. Burrows
Merithew Hills

ADMINISTRATION AND SERVICES

GROUP 60

Proctor, J. C., Leader

Biagiotti, R.
Brock, S. T.
Essler, G.
Falcione, A. M.
Ferguson, M. M.
Hazel, F. P.
Heidler, G. R.
Hodgdon, H. W.
Kates, W. A.
Morley, H. B.
Morrione, C., Jr.
Smith, A. R.

VIII. ADMINISTRATION AND SERVICES
GROUP 60

A. SUMMARY

The main activity of Group 60 is of a supporting nature. The general engineering section, furnishing design service and shop facilities to Division 6 and other divisions, reports the following work as being particularly noteworthy.

Three devices were designed to facilitate the development of experimental computers. A tape reader for punched paper tape was designed which should prove to be faster, more reliable, and more convenient to use than commercially available readers. A potentiometer of unique construction was made for the purpose of testing power transistors with a high degree of accuracy. An automatic machine which strips insulation from the fine wire used in miniaturized memory planes was put into successful operation.

J.C. Proctor

B. GENERAL ENGINEERING

1. High-Speed Tape Reader for Computer Inputs

A new reader for punched paper tape has been designed which should prove to be faster, more reliable, and easier to use than existing equipment. Read-in speed is 40 inches/sec, 60 per cent faster than existing machines. Photodiodes replace phototransistors for greater reliability. A take-up device, still in the process of refinement, will collect the tape in a manner which will make it easier to handle and to store.

2. High Resolution Potentiometer for Testing Power Transistors

Power transistors can be tested more accurately with a potentiometer which combines high resolution with relatively large (1 amp) current-carrying capacity. A long unwieldy wire, tapped with alligator clips, has been the only method that has satisfied these two requirements.

In a new design (Fig. 60-1) the long wire is replaced by a resistance ribbon which is wound on a pair of in-line reels. To make the voltage measurement, the operator winds the tape to "balance" position by means of a crank mechanism of unique design. Single-drive point operation is achieved, constant tape tension is maintained, and slack is taken up by means of a spring-loaded differential in the mechanical linkage between reels.

3. Log Cameras for Kingston

At the request of Group 66 a log camera installation for each of the three test areas at Kingston, has been designed. When installed, the cameras will photograph the neon tube array whenever the computer fails. Having thus recorded the panel display, the operator can return the computer to service in a relatively short time (usually less than two minutes); the photographic prints serve as the record of computer operation and can be studied later by programmers.

4. Automatic Wire-Stripping Machine

The miniaturization of components for experimental computers has introduced several new problems in design. One such problem was solved during the quarter by the design of a

GROUP 60

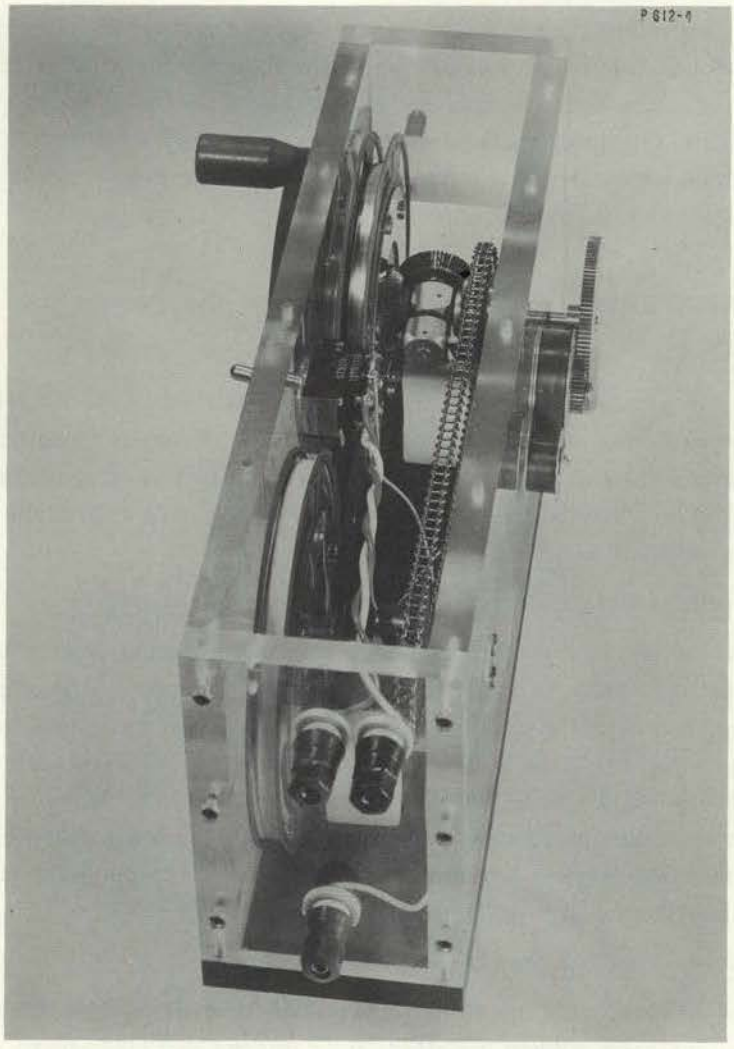

Fig. 60-1. High-resolution potentiometer.

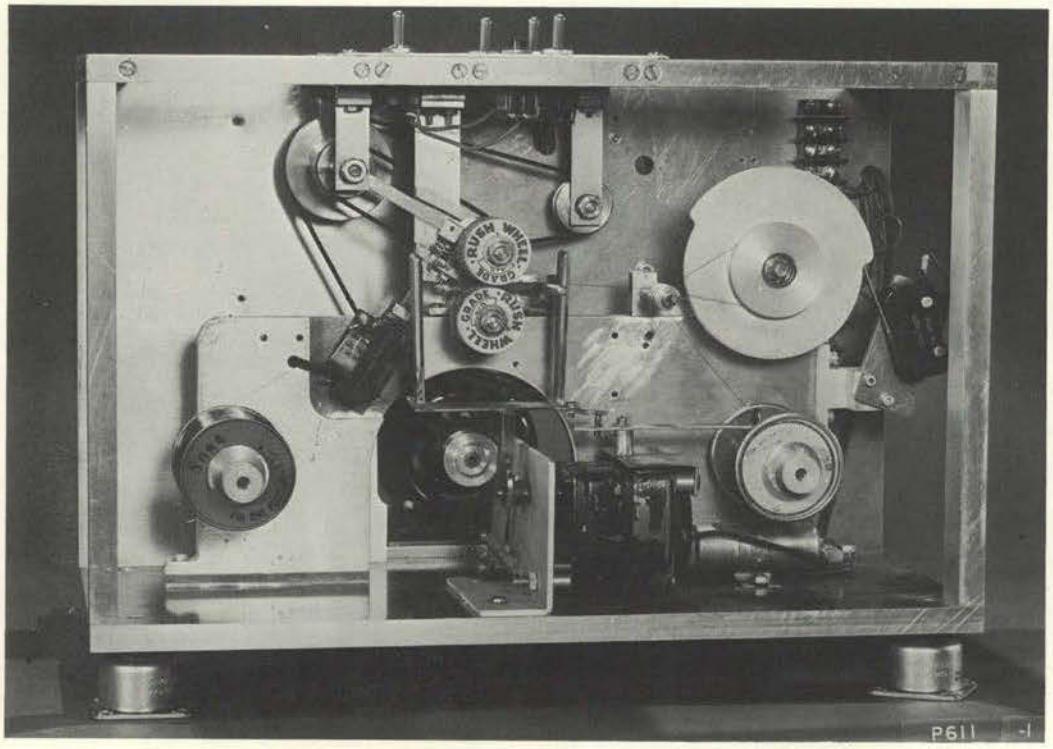

Fig. 60-2. Automatic wire-stripping machine.

power-driven machine for stripping insulation from fine copper wire (see Fig. 60-2). Wire as small as 0.005" is used in memory planes having 30-mil by 50-mil ferrite cores. Whereas previous techniques had called for a length of the wire to be cut to size before stripping, the new machine automatically removes predetermined lengths of insulation from the wire as it is wound from one spool to another.

A. R. Smith
G. Essler
G. R. Heidler

UNCLASSIFIED

APPENDIX 63-A

THE LINCOLN TX-2 COMPUTER

UNCLASSIFIED

APPENDIX 63-A
THE LINCOLN TX-2 COMPUTER

ABSTRACT

The information contained in this report was presented at the Western Joint Computer Conference held at Los Angeles, California, in February 1957. The papers given form the sections of this memorandum and are as follows:

THE LINCOLN TX-2 COMPUTER DEVELOPMENT
by Wesley A. Clark

Construction of the TX-2 computer at the Lincoln Laboratory of M.I.T. is part of the Lincoln program for the study and development of large-scale digital computer systems. The Lincoln TX-2 incorporates several new developments in high-speed transistor circuits, large capacity magnetic-core memories, and flexibility in machine organization and is designed to work efficiently with many input-output devices of different types. In the course of development of the TX-2, Lincoln has constructed a small self-checking multiplier system which is on life test, and a complete, though skeletal, general-purpose computer known as the TX-0 which is now in operation.

A FUNCTIONAL DESCRIPTION OF THE LINCOLN TX-2 COMPUTER
by John M. Frankovich and H. Philip Peterson

The Lincoln TX-2 computer is a general-purpose, binary parallel machine with a code of 64 single-address instructions and 64 index registers. The design provides for a random-access memory of 260,000 36-bit words. The instruction code includes the usual arithmetic and logic operations executed at a peak rate of 160,000 36-bit additions per second, with several interesting variants. A unique feature of the central computer is its ability to deal with operands in one 36-bit, one 27- and one 9-bit, two 18-bit, or in four 9-bit configurations. These configurations are specified by each instruction – a feature which permits the 9-bit quarters of the arithmetic element to be connected in various ways to the corresponding quarters of the memory. Control is exercised over the activity of the quarters during the execution of the instruction.

THE LINCOLN TX-2 INPUT-OUTPUT SYSTEM
by James W. Forgie

The Lincoln TX-2 computer design uses the "multiple-sequence program technique" to permit the concurrent operation of a number of input-output devices. A stored program (instruction) counter is associated with each input-output device. The programs referred to by these counters time-share the hardware of the central computer, giving attention to the associated input-output devices as required. A priority system ranks the devices according to speed and type for efficient operation with a minimum of programming restrictions. The multiple-sequence program

technique provides an environment in which buffer storage may be considerably reduced at a small cost in machine speed within the limits set by peak and average data rate considerations.

MEMORY UNITS IN THE LINCOLN TX-2
by Richard L. Best

There are three random-access core memories in TX-2 – all of which may be operated independently and concurrently. Two of these are for conventional storage of data and instructions. The third is used as a file of index registers and program counters. The three types of core memories in TX-2 are described. The largest memory contains 65,536 words 37 digits long, and has a full cycle time of 6-1/2 μsec. The next largest is entirely transistor driven, contains 4,096 words, 37 digits long, and has a 6-μsec cycle time. The smallest and fastest contains 64 words, 19 digits long, and uses external selection and two cores per bit to achieve a "read" cycle time of 1 μsec and a "write" cycle time of 3 μsec. Ferrite cores only 0.050 inches O.D. are used in the two smaller memories.

TX-2 CIRCUITRY
by Kenneth H. Olsen

Only two basic transistor logic circuits are used in TX-2. Surface barrier transistors in saturated emitter-follower circuits are grouped in parallel for "AND" "OR" operations; groups of inverter circuits are connected in series, parallel, or series-parallel to perform more complicated logic operations. The TX-2 flip-flop is assembled from saturated inverters and emitter-followers and incorporates enough amplification so that it appears to the logic designer as a simple switch over a wide range of loads.

Circuit tolerance to variations in transistor and other component characteristics, in temperature, supply voltages, and noise was studied in detail and designs were adjusted to minimize the effects of them. The study led to the selection of voltage-sensitive parameters for indicating the deterioration of components with age and became the basis of the marginal checking system.

ACKNOWLEDGMENT

We are indebted to Mr. Frank P. Hazel and Miss June Karlson for their assistance in editing; to Mrs. Barbara Clark, Miss Carole Olson, Miss Elaine Tonra and Miss Ruth McDonald for their typing of the manuscripts; and to Miss Alice Griffin and her associates for the preparation of the many figures.

I. THE LINCOLN TX-2 COMPUTER DEVELOPMENT

A. INTRODUCTION

The TX-2 is the newest member of a growing family of experimental computers designed and constructed at the Lincoln Laboratory of M.I.T. as part of the Lincoln program for the study and development of large-scale, digital computer systems suitable for control in real time. Although, in general characteristics and design philosophy, it owes a great deal to its predecessors, Whirlwind I and the Memory Test Computer, the Lincoln TX-2 incorporates several new developments in components and circuits, memories, and logical organization. It is the purpose of this paper to summarize these new features and to give some idea of the historical development and general design objectives of the TX-2 program. Figure 1 shows TX-2 in its present development stage.

Fig. 1. The Lincoln TX-0 and TX-2 computers.

Foreground:	TX-0 console
Middle center:	TX-0 central computer frame
Right rear:	Partially completed TX-2 frame showing plug-in unit construction
Left rear:	The 256 × 256 memory

B. HISTORY

With the development by Lincoln and IBM engineers of the SAGE computer for air defense, real-time control computer systems had reached an impressive level of size, sophistication, and complexity. The highly successful 64 × 64 coincident-current, magnetic-core, memory array was in operation in the Memory Test Computer which had given up its earlier 32 × 32 array to Whirlwind. Vacuum tubes abounded in all directions. It was apparent that the further advances

in system design which could be made by increasing memory size, eliminating vacuum tubes wherever possible, and organizing input-output buffering, control, and communications into more efficient forms, would be well worthwhile.

The development of a 256 × 256, switch-driven, magnetic-core memory array was begun and the Philco surface-barrier transistor made its appearance. After some very promising bench experiments with flip-flops and logic circuits, it became apparent that this transistor was potentially well-suited to use in large-scale systems and warranted further study. Accordingly, plans were laid for a succession of experimental digital systems of increasing size and complexity which would make possible the development and evaluation of circuits using the surface-barrier transistors, and which would lead to a computer of advanced design that would be capable of making efficient use of the 256 × 256 memory.

A double-rank shift register of eight stages and containing about 100 transistors was constructed and put on life-test in April 1955. It has since been circulating a fixed pattern almost continuously with no known errors and no natural transistor failures.

As the next step, it was decided to build a small, high-speed, error-detecting multiplier and incorporate marginal checking and other system features. The value of a multiplier as a preliminary model had been well demonstrated by the 5-digit system built during Whirlwind's early development. The shift, carry, count, and complement operations, under closely controlled timing conditions, were felt to be representative of all of the operations in the manipulative elements of the type of computer planned. Accordingly, an 8-bit system using 600 transistors was designed and completed in August 1955 and has been in nearly continuous operation since. Operating margins are periodically checked, and in steady state operation, the multiplier's error-rate has been about one every two months or one error per 5×10^{11} multiplications at 10^5 multiplications per second. Most of these errors appear to have been caused by cracks in the printed wiring which open intermittently.

During this period, a better idea of the general characteristics of the projected computer began to develop and the engineers who were designing the 256 × 256 memory were encouraged to think in terms of a word of 36 bits. The notion of a logically separate input-output processor was examined and rejected in favor of a minimum buffering scheme in which data is transferred directly to and from the central memory of the computer. The possibility was recognized of programming these transfers by means of additional program sequences and associated program counters, thus taking advantage of the extensive facilities of the central machine itself for processing input-output data.

It was realized that another development step was desirable before attempting such an elaborate 36-bit system. The 8-bit multiplier had produced a certain measure of confidence and familiarity with circuits, packaging, and techniques of logical design, but there remained the problems associated with communicating with memory units and input-output equipment operating at vacuum-tube levels over relatively large distances from a central machine which operated at transistor levels. It appeared that the memory development, which had now entered the construction phase, would also benefit by a preliminary evaluation of the 256 × 256 array and its switching, timing, and noise problems in an operating computer of some kind, possibly with a reduced word

length. It was, therefore, decided to design and build next a simple machine – in fact, the simplest reasonable machine – in order to bring about an early intermediate closure of the various efforts within the program.

After some thought about the various possible minimal machines, a design was completed in which the word length would be 18 bits – a graceful half of the projected final form. We began to refer to this computer as the TX-0 and to the projected machine as the TX-2. Because the 256 × 256 memory array required 16 bits for complete addressing, the single-address instruction word of the TX-0 was left with 2 bits in which to encode instructions. The particular set of instructions chosen included three which required a memory address (add, store, and conditional jump) and one which did not. In this last instruction, the remaining 16 bits were used to control certain necessary and useful primitive operations such as clearing and complementing the accumulator, transferring words between registers, and turning on and off input-output equipment.

The TX-0, equipped with a Flexowriter, a paper-tape reader, and a cathode-ray tube display system was completed, except for the memory, in April 1956. Twenty planes of the 256 × 256 memory array were installed the following August and the TX-0, now containing about 3600 transistors and 400 vacuum tubes, began to function as a complete computer. Since that time, it has been used to run a variety of testing and demonstration programs, and a symbolic address compiler and other utility programs have been constructed and are currently in use.

Not only has the TX-0 served the evaluational purposes for which it was built, but it has also demonstrated an effectiveness as a usable computer that is somewhat surprising in view of its simplicity. Its relatively high speed of about 80,000 instructions per second and its 65,536-word memory compensate in large measure for the limitations of its instruction code and logical structure.

With the successful completion of the TX-0, the final steps in the development were undertaken in packaging, circuit refinement, and logical design of the TX-2. A great deal had been learned about the performance of the transistors and memory, the types of logical circuits which are practical, techniques of marginal checking, and the lesser system problems such as color scheme selection and the proper location of pencil sharpeners. As design work progressed, the TX-2 took form as a system of about 22,000 transistors and 600 vacuum tubes. It is an interesting fact that at each step of the development since the shift register, the number of transistors involved was about 6 times the number in the preceding step. This is graphically shown in Fig. 2. At the time of writing approximately 16 million transistor-hours have accumulated in the shift register, multiplier, and TX-0. There have been two natural deaths and a dozen or so violent ones, primarily due to contact shorting with clip leads and probes.

C. DESIGN OBJECTIVES

In describing design objectives, it should be pointed out that speed of operation was <u>not</u> the primary consideration to which all other attributes were sacrificed. It would have been possible, at the expense of a few more logic circuits, to increase the speed of multiplication, division, and shift-type operations. Similarly, the operation of the index register system could have been made more efficient at the cost of an additional small, fast memory. The principal objective

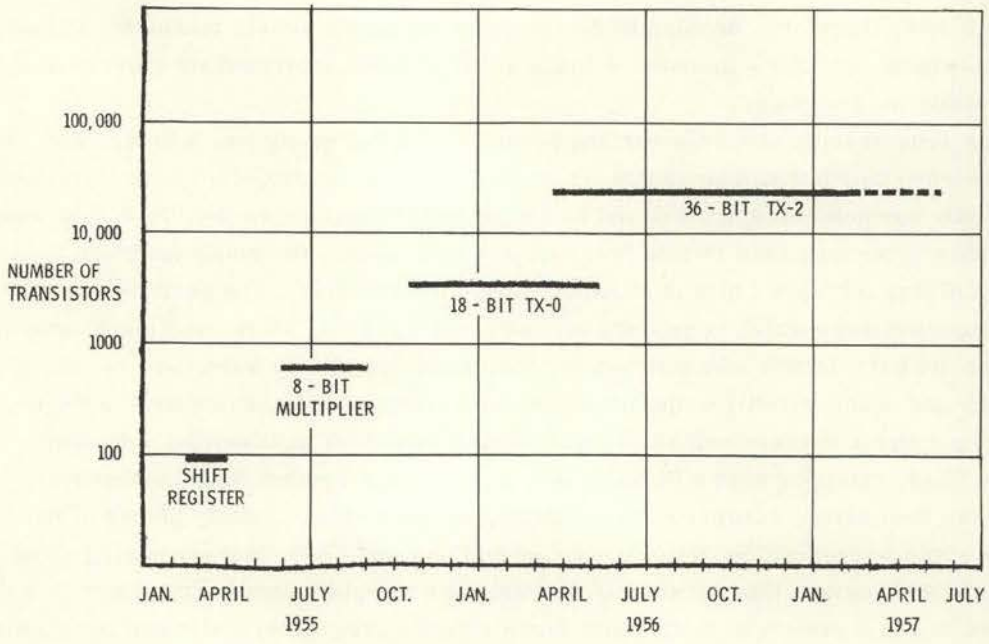

Fig. 2. Steps in the Lincoln TX-2 development program.

was rather that of achieving a balance between the factors of speed, reliability, simplicity, flexibility and general virtue.

A key aspect is that of expandability which, in an experimental computer in an active environment, certainly ranks with the foregoing qualities in importance. The address structure in the TX-2 permits an expansion of the memory by about a factor of 4, partly to allow for new memory developments, such as the transistor-driven 64 × 64 array which was begun following the completion of TX-0. New instructions and pieces of terminal equipment will certainly be added during the course of future operation. Extra space and spare plugs have been artfully distributed about in constructing the computer frame. Finally, modular construction will permit a fairly easy physical expansion when required.

The result of all this activity has been a computer of relatively large capability. In addition to incorporating high-speed transistor circuits and a large magnetic-core memory array, the Lincoln TX-2 has two major and distinguishing design characteristics:

1. The structure of the arithmetic element can be altered under program control. Each instruction specifies a particular form of machine in which to operate, ranging from a full 36-bit computer to four 9-bit computers with many variations. Not only is such a scheme able to make more efficient use of the memory in storing data of various word lengths, but it also can be expected to result in greater over-all machine speed because of the increased parallelism of operation.

   Peak operating rates must then be referred to particular configurations. For addition and multiplication, these peak rates are given in the following table:

PEAK OPERATING SPEEDS OF TX-2

Word Lengths (in bits)	Additions per second	Multiplications per second
36	150,000	80,000
18	300,000	240,000
9	600,000	600,000

2. Instead of one instruction counter, the TX-2 has 32 such counters which are assigned separately to different users of the computer, who then compete for operating time from instruction to instruction. A special part of the machine selects a particular user based partly on a predetermined priority schedule and partly on the current needs of that user. This multiple-sequence operation, in which many essentially independent instruction sequences interrupt and interleave one another, is an extension of the breakpoint operation found in DYSEAC of the National Bureau of Standards.

The value of these features will have to be assessed during the course of future machine operation. The features themselves are discussed in more detail in the following sections of this report.

II. A FUNCTIONAL DESCRIPTION OF THE LINCOLN TX-2 COMPUTER

A. INTRODUCTION

TX-2 is a large-scale digital computer, designed and built at the MIT Lincoln Laboratory, which uses new memory and circuit components and some new logical design concepts. The computer will be a research tool in scientific computations, data-handling, and real-time problems. The design of the computer reflects not only the characteristics of the components available, but also the nature of the intended applications. This section describes the functions and organization of the computer that are important from the user's point of view.

B. GENERAL STRUCTURE OF TX-2

TX-2 is a parallel, binary computer with words 36 digits long. The internal memory is random-access and will initially consist of 69,632 registers of parity-checked, magnetic-core memory and about 24 additional toggle-switch and flip-flop registers. About 150,000 instructions can be executed per second. Instructions are indexed, single-address type and a fixed-point, signed-fraction, ONE's-complement number system is used.

Several unusual ideas incorporated in the organization of the system reduce the amount of information unnecessarily manipulated during program sequences. Furthermore, the organization facilitates the execution of several operations simultaneously, thereby increasing the effective speed of the computer.

The principal registers and information paths in the computer are illustrated schematically in Fig. 3. A, B, C, D, E, F, M, and N are the 36-bit flip-flop registers in the machine. M and N are memory buffer registers, each of which has a parity flip-flop and associated circuitry used to check the parity of memory words. P, Q, and X are 18-digit registers; X also has a parity digit which is used to check the parity of words in the X-memory. Control flip-flops are not shown in Fig. 3.

Instructions are full memory words and are placed in the control element during the instruction memory cycle. During the operand memory cycle, an operand is usually transmitted between the memory element and some other element – always through the exchange element. The 36-digit configuration of the memory is not, however, maintained throughout the computer during operation timing. A programmer can, in effect, simultaneously control several independent computers with operands of shorter word lengths during the execution of each instruction. This flexibility is realized by specifying a particular system configuration with each instruction.

The computer communicates with the outside world through units in the in-out element, several of which can be simultaneously operated. Whenever any piece of data (input or output) is ready to be transferred between an in-out unit and a register in the memory element, signals to the program element from the in-out element automatically call into operation the instruction sequence associated with the in-out unit. This process is referred to as multiple-sequencing and will be described in Section III of this report.

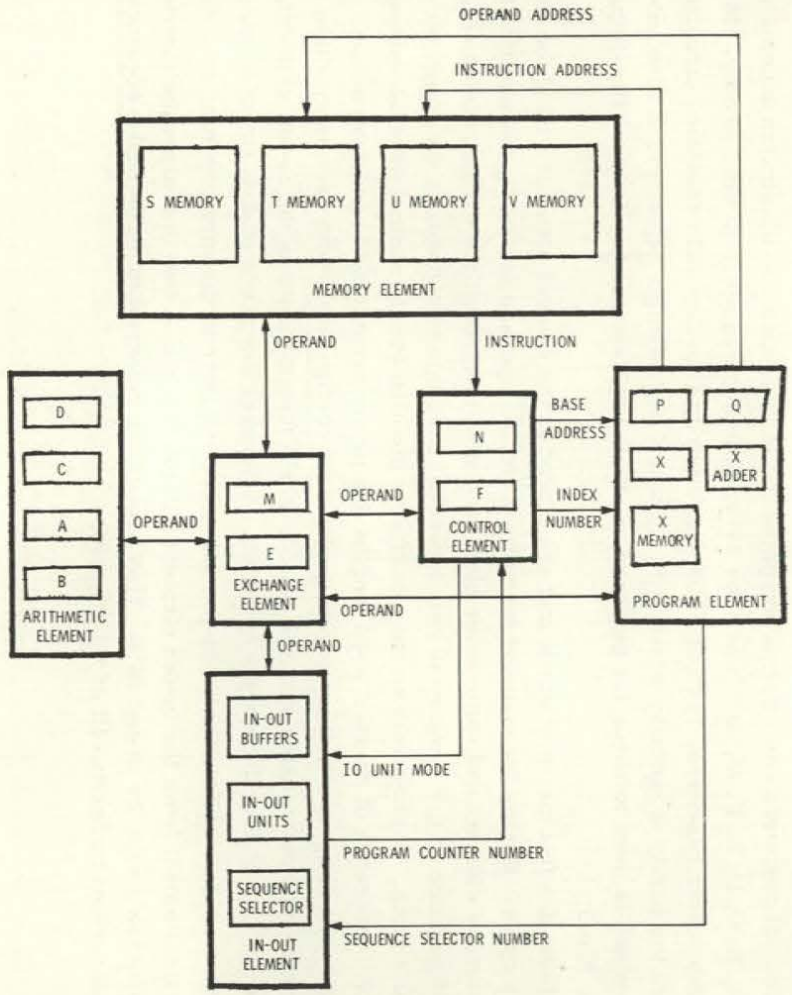

Fig. 3. TX-2 system schematic.

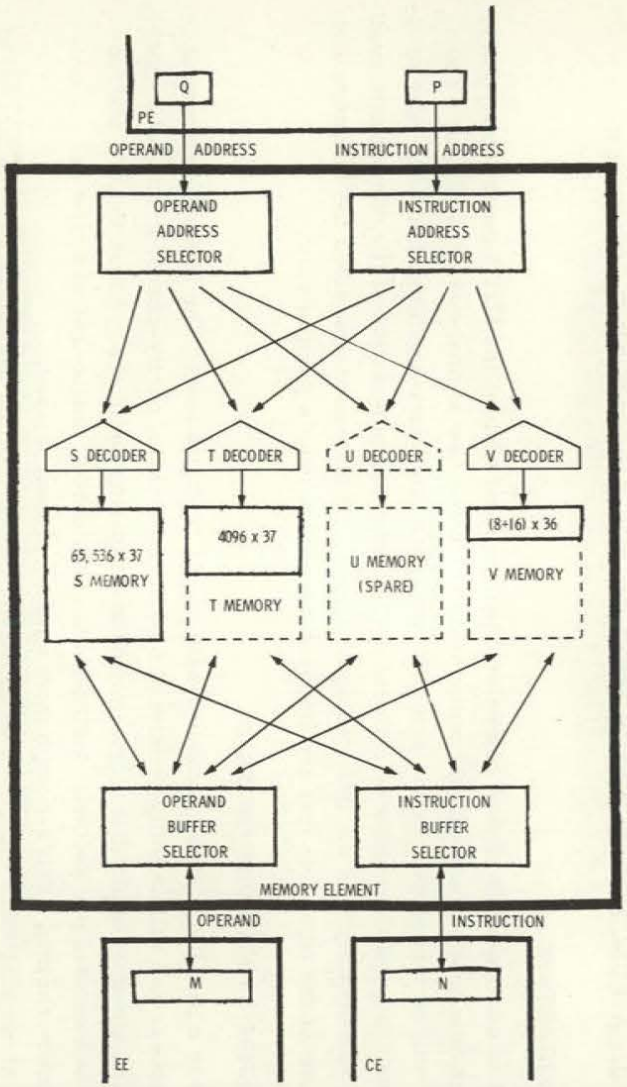

Fig. 4. TX-2 memory element, showing method of using two address registers and two buffer registers to simultaneously operate two out of four memories.

C. MEMORY ELEMENT

The availability of a large, fast, core memory for TX-2 permitted an emphasis on the design of a machine with a completely random-access memory with a design capacity of 262,144 words. The homogeneous aspect of such a large memory system simplifies the programmer's coding problems and permits continued high-speed operation regardless of where the program is located in the internal memory.

The TX-2 memory element (Fig. 4) is divided into four independently operating memory systems, each containing up to 65,536-digit words. The operating speed of TX-2 is determined by the cycle time for the memories: The 65,536-word S-memory is expected to have a cycle time of between 6.0 and 7.0 μsec, and the 4,096 T-memory, a cycle time between 5.0 and 6.0 μsec. Both memories have parity checks.

Although the U-memory is not presently specified, it may contain a 4,096-word core memory in the initial system. The V-memory consists of 8 flip-flop registers in the central machine and 16 toggle-switch registers which contain the program sequence executed whenever the START button on the operator's console is pushed. The contents of the toggle-switch registers can be used as instructions or operands, but cannot be altered by a program. The six 36-bit registers A, B, C, D, E, and F are part of the V-memory, but their contents can be used only as operands during the execution of an instruction. The programmer has, in a limited sense, a two-address instruction machine when he refers to these registers in load and store type instructions. The other two flip-flop registers in the V-memory are a 60-cps clock and a random-number register.

When an instruction calls for the storing of an operand in memory, the operand memory cycle can be extended up to 2.0 μsec. The extension occurs between the time that the memory register is read and the time that it is rewritten. During this extension, the contents of memory registers in the central computer are transferred, the parity of the word read from memory is checked, and the parity of the new memory word is computed. Because the extended cycle is less than the two complete cycles usually used for instructions that modify words, computing efficiency is increased.

The P-register in the program element specifies the location of an instruction in memory and the N-register in the control element holds the instruction after it has been read from memory. The first 2 digits (reading left to right) of P select the memory system from which the instruction word is to be obtained; the remaining 16 digits address the word within the memory. Similarly, the Q-register locates the operand in one of the memory systems, and the operand is placed in the M-register.

D. CONTROL AND INDEXING

An instruction word read into N has the structure shown in Fig. 5. The first 2 digits of the word specify information to the in-out element, and the 4 cf digits specify the computer configuration. The interpretation of the b and n digits is discussed in Section III. The cf digits are discussed in subsection H.

The operation code for the instruction is specified by the 6 op digits. On simple load and store type instructions, these 6 digits are further subdivided into two groups of three. The first

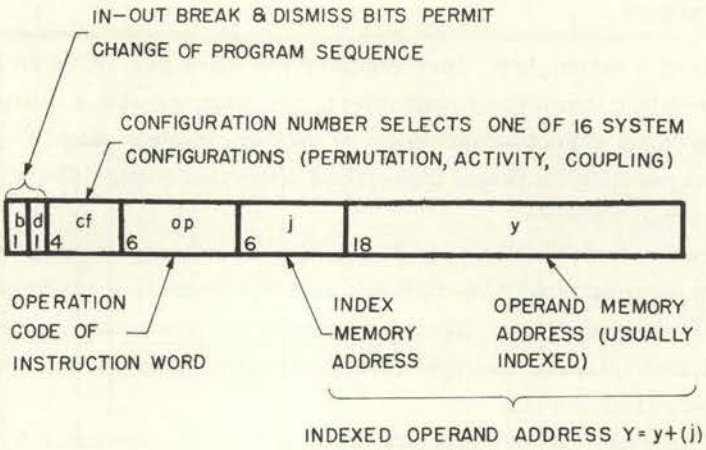

Fig. 5. TX-2 instruction word structure.

group determines the operation and the second specifies the register in the central computer that is being loaded, or whose contents are being stored.

The base address for the operand, formed by the 18 y-digits, is usually modified by the contents of the index register selected by the 6 j-digits. The index registers form a unique, 64-register, parity-checked, core memory which has an access time of 1.0 μsec. The contents of the specified index register is read into the X-register of the program element via the paths indicated in Fig. 6. The base address and the index are fed into a full adder circuit which produces the sum, X = y + (j), in about 1.0 μsec. The over-all complexity of the program element was reduced by having the adder produce both the sum, Y, and the unmodified base address, y: either of these quantities can be directed to the operand memory address register, Q. Whenever the FIRST (j = 0) index register is chosen, the adder produces only the unmodified base address. The effect is the same as having that index register contain ZERO and the programmer can avoid index modification altogether.

The P-register, which holds the memory address of instruction words, normally is indexed by one as each instruction is executed, but the output of the index adder is sometimes directed to P when jump instructions are executed. The adder also provides a communication path for index jump instructions from the X-memory to the memory element by way of the exchange element.

E. ARITHMETIC ELEMENT (AE)

Figure 7 shows the registers and sufficient basic operations in the arithmetic element for adding, multiplying, dividing, shifting, and executing various logic instructions. Operation timing for most of the TX-2 instructions is also performed in the arithmetic element.

The design of the AE reflects the desire to attain high-speed operation for TX-2, even when the AE is carrying out lengthy instructions. The only instructions which take longer than one memory cycle for execution are those which involve shifting. These are, for example, multiplication, division, arithmetic and cyclic shifting, and normalization. Therefore, the AE

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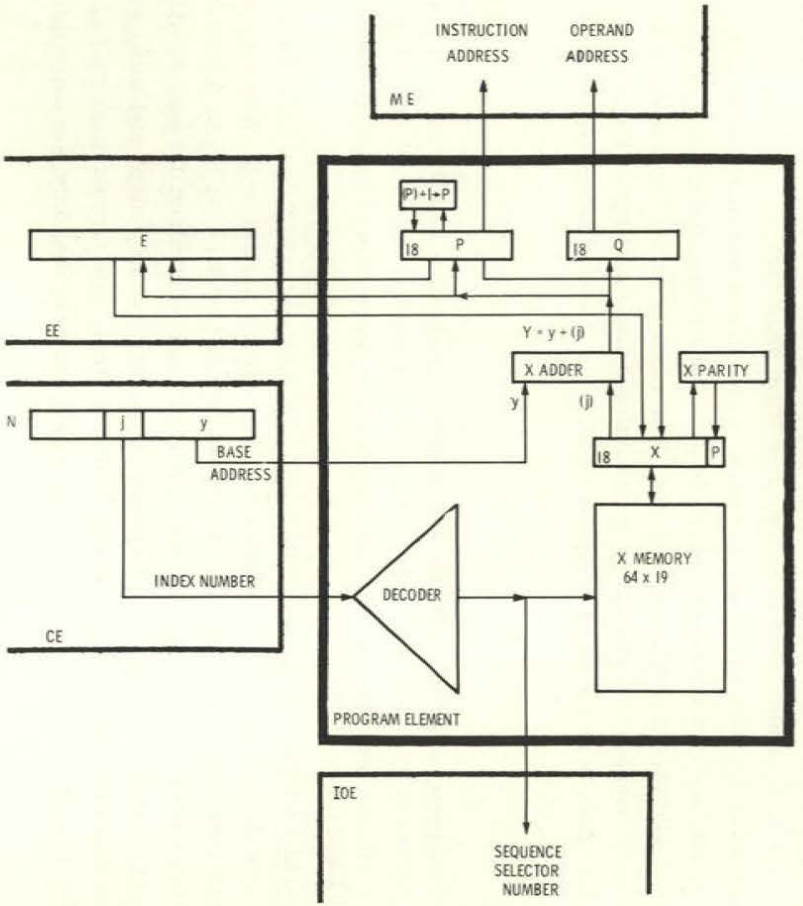

Fig. 6. Program element, showing paths enabling index adding and storing and loading program counter from the index memory and the exchange element.

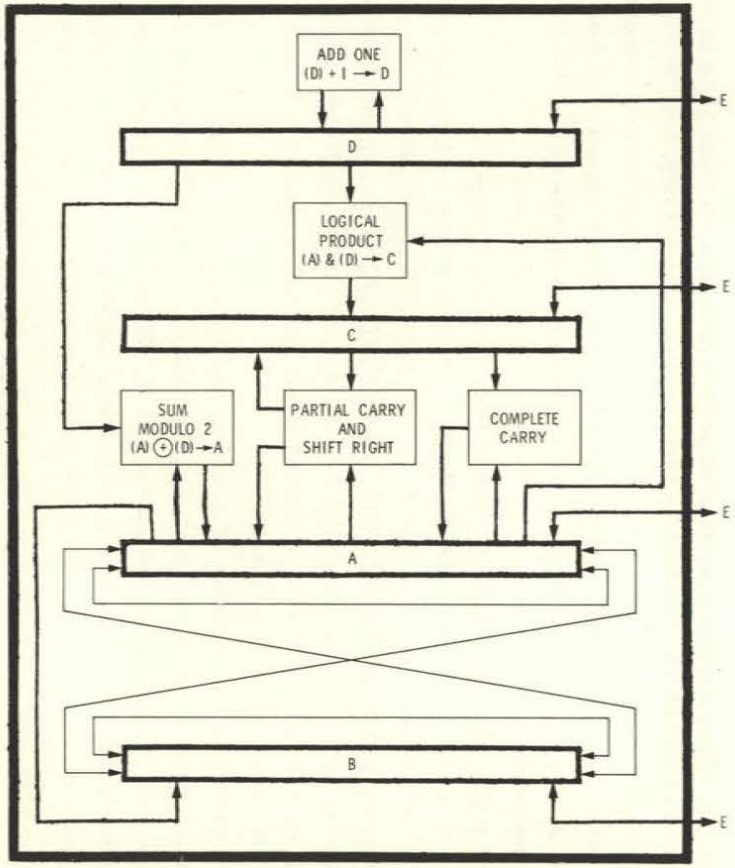

Fig. 7. Circuits and transfer paths (general) of any TX-2 arithmetic element forms.

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contains a sufficient number of storage registers to permit these instructions to be carried out in the AE while the remainder of TX-2 is free to execute other instructions.

The four registers in the AE can each communicate with the E-register in the exchange element and thus with the memory element. As mentioned earlier, these registers are addressable as part of the V-memory system. Therefore, programmers have access to the results in any register of an AE computation.

The AE registers, designated by A, B, C, and D, are described below:

The A-Register accumulates the results of all the arithmetic operations, except division, for which it holds the remainder. It holds one of the operands and accumulates the results of the three logic operations (AND, INCLUSIVE OR, EXCLUSIVE OR) which, it should be noted, are bit-wise operations. The information in the A-register can also be shifted (i.e., multiplied by some positive or negative power of two) or cycled (i.e., shifted, without preserving the special significance of the sign bit, as in a closed ring).

The B-Register serves as an extension of A during multiplication, certain shifts and cycles, and, in a sense, during division when the least significant digits of the double-length dividend are stored in B. The resulting quotient then appears in B. Moreover, the information in B can be shifted or cycled independently of A. In multiplication, the multiplier originally in A is transferred via parallel paths directly into B (where the least significant digit then controls the operation).

The C-Register stores the partial carries during arithmetic operations, which is most important during multiplication, as described later. Since these partial carries are actually bit-wise logic products AND, C is also used to accumulate logic products.

The D-Register holds the multiplicands, divisors, addends and one of the operands for the logic operations. It also holds the numbers which control the shifting and cycling of A and B, namely the number of places, up to 62, and the direction, right or left. The ability of D to count is used also to accumulate the results of normalizing A and counting ONES in A.

Each of the AE registers can also be complemented, thus allowing subtractions to be performed.

F. AE CIRCUITS

There are four add-one circuits on D, so that different parts of A and B can be controlled separately and simultaneously. For simplicity, just one add-one circuit is shown in Fig. 7. These add-one circuits use the simultaneous carry principle, permitting one count every 0.4 μsec; each can count up to 127.

The logical-product (AND) circuit of A and D into C and the sum-modulo 2 (EXCLUSIVE OR) circuit of A and D into A when used at the same time are called a partial add. When the complete-carry circuit is activated after a partial add, the result is a full addition of D and A into A. The complete-carry circuit uses the high-speed carry principle and takes about 1.5 μsec for 36 bits.

The partial-carry and shift-right circuit is also known as "multiply step" and was, we believe, first used on Whirlwind I. As it is used in multiplication, this circuit makes a full addition unnecessary for each ONE in the multiplier. Carries are extended only one stage during

each step, except the last, when a complete carry is executed. The complete process takes about 16 μsec at most for a full, 36-digit multiplication. The process for division, on the other hand, requires a complete addition at each step and consequently takes about 72 μsec in the worst case.

Two features of the AE control should be mentioned here. A 7-bit step counter, like the add-one circuit on D, controls multiplication and division and limits the shifting in normalizing and the cycling in counting ONE's. A flip-flop, which signifies overflow during addition and division, is also used to remember the sign of the product during multiplication and the sign of the quotient during division. If division causes an overflow, the sign is replaced by the overflow state and the quotient is lost.

Control of the arithmetic element is independent of the rest of the machine. Thus, non-AE instructions can be executed while the AE continues to perform a long shift operation or a division.

G. SYSTEM TIMING

The high speed of TX-2 is attained in part by overlapping the operation of as many components as is logically possible without incorporating large amounts of circuitry. The time-consuming cyclic operations in an indexed, single-address computer are the instruction memory cycle, the index memory cycle, the index addition time, the operand memory cycle, and the operation timing. These cycles occur in the mentioned sequence during the execution of ordinary instructions. Several asynchronous "clocks," which use a 5-megacycle pulse-source, control the cycles. The instruction and operand memory cycles can be overlapped if they take place in different memory systems.

The overlap of these cycle times for a sequence of load-type instructions is illustrated in Fig. 8(a). Here different instruction and operand memory systems are assumed to have roughly equal cycle times. If a sequence of store-type instructions is executed which requires extended memory cycles for the operands, then the situation is as shown in Fig. 8(b). Figure 8(c) shows the time used when both the instruction and the operand are in the same memory.

"Peak" operating speed for the computer is attained only when the situation is as shown in Fig. 8(a); in the situation shown in Figs. 8(b) and 8(c), the operating speed could be increased by adding circuitry, but only at considerable cost. It is interesting to note that if the computer is to run at peak speeds, the address of the operand used by the present instruction must be available before the earliest moment at which the next instruction memory cycle could begin. If the total accumulated time, from the beginning of an instruction memory cycle till the time that the address of the operand is known, is greater than the instruction memory cycle time, then the computer cannot run in the ideal manner shown in Fig. 8(a). This means that the access time of memories and the index-add time must be kept as short as possible.

Figure 8(d) shows the timing of events when the in-out element causes a change in program sequence by changing the contents of the P-register. The additional X-memory cycle, which must be performed, produces a timing situation similar to that of the X-memory load and store instructions.

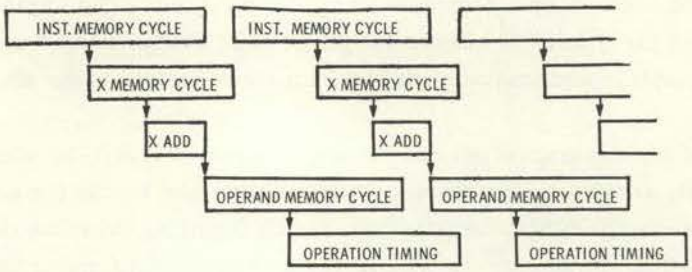

Fig. 8(a). Consecutive load type instructions and operands in different memories.

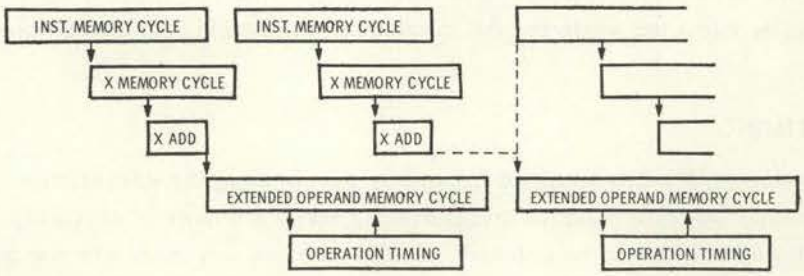

Fig. 8(b). Consecutive store type instructions.

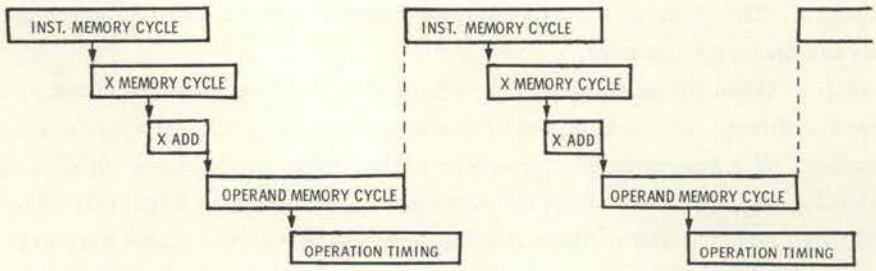

Fig. 8(c). Instruction and operand in same memory.

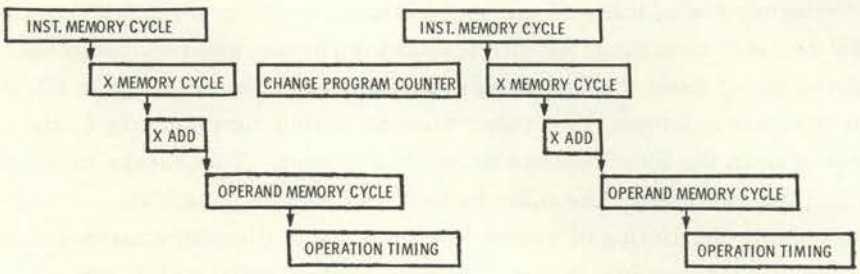

Fig. 8(d). Change sequence.

The operation timing for an instruction is executed when the operand is available from memory. Only the arithmetic element step-counter instructions (multiply, divide, shift, etc.) require an operating timing cycle longer than a memory cycle. Since only the arithmetic element is tied up by these instructions, the control element permits any non-arithmetic element instruction to be executed while the AE is busy. Division takes up to 75 μsec, so the programmer can write as many as 14 non-AE instructions following a divide, all of which can be executed before the division is completed.

H. CONFIGURATION CONTROL

The design of a general-purpose computer must necessarily reflect the contradictory demands for both short and long words, floating and fixed-point arithmetic operations, and a multitude of logic and decision instructions. The computer should be able to process information at an optimum rate, in a variety of problems, without the need for intricately coded programs. This ability should be achieved without excessively complex and costly circuitry.

The 36-digit word of TX-2 represents a reasonable length for operands in some numerical computations, notably scientific and engineering computations. Though floating-point arithmetic operations are not included in the instruction code, both they and multiple-precision operations can be easily synthesized by means of the existing instructions. The logic instructions in the code facilitate operations on individual digits. Also, a configuration which the programmer specifies with each instruction permits him to perform arithmetic operations on operands that are less than 36 digits long. When operands are less than 36 digits, several can be manipulated simultaneously.

The four cf digits in an instruction word (see Fig. 5) are decoded as shown schematically in Fig. 9, selecting one of 16 configurations. The selected configuration, represented by a 9-digit word, is placed in a flip-flop register whose output levels determine a static configuration for the entire computer while the instruction is executed. The notation used to represent the contents of the first 12 registers will be clarified in the following discussion.

The full 36-digit word length is always maintained for instruction words, but during operation timing, every 36-digit register in the memory, exchange and arithmetic elements is considered as broken into 9-digit quarters, numbered from 1 to 4, right to left, as in Fig. 10(a). While the instruction is being executed, these quarters are recombined on the basis of the configuration.

Information is usually moved about in the machine by parallel transfers between registers (see Fig. 9). The EE permutation digits select one of the four permutations P0, P1, P2, P3, shown in Fig. 10(b). The chosen permutation effects the corresponding cross-communication paths between the quarters of the E- and M-registers of the exchange element. While operands are transmitted through the EE, the quarters follow the set of paths determined by the selected permutation. The result is that the operand is shifted 9n places to the left as it moves from M to E or 9n places to the right as it moves from E to M, n = 0, 1, 2 or 3. Thus, the programmer can have any quarter of the AE communicate with any quarter of the ME.

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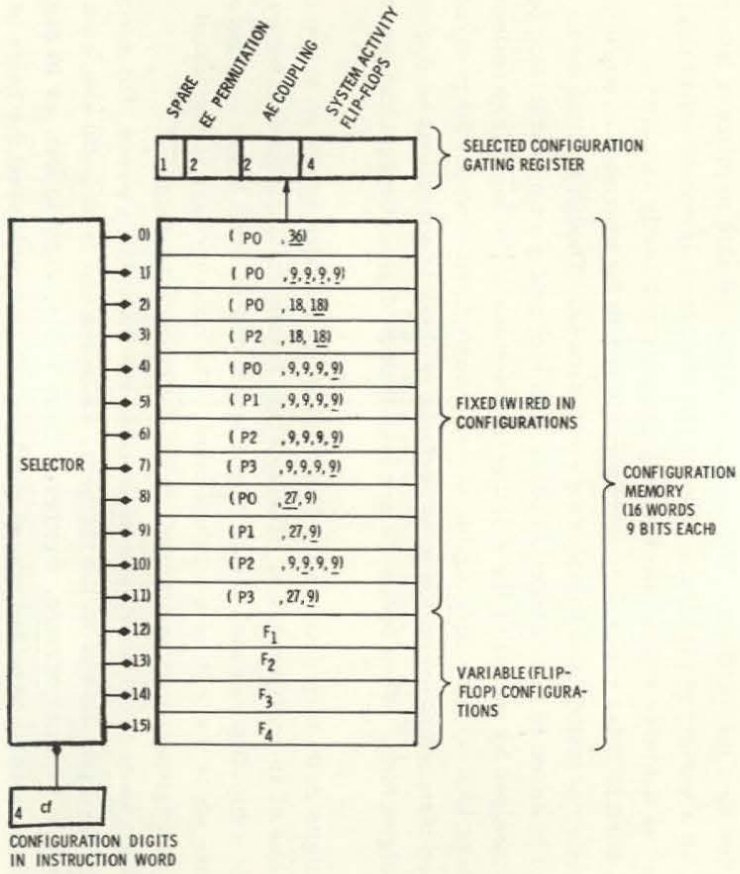

Fig. 9. TX-2 configuration selection.

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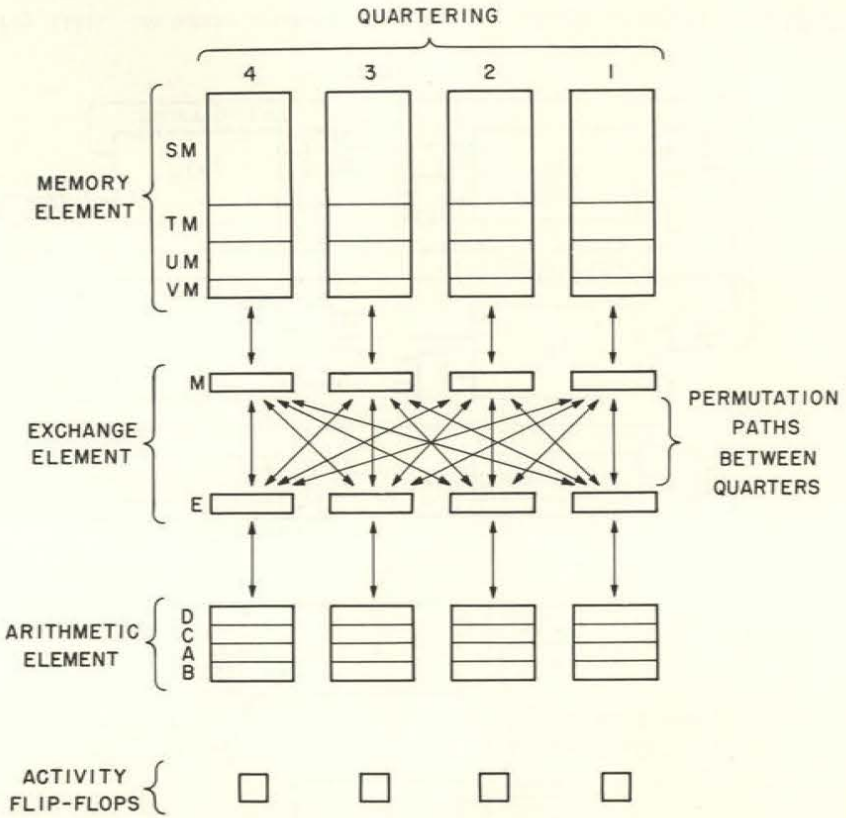

Fig. 10(a). Quartering permutation paths and activity flip-flops shown.

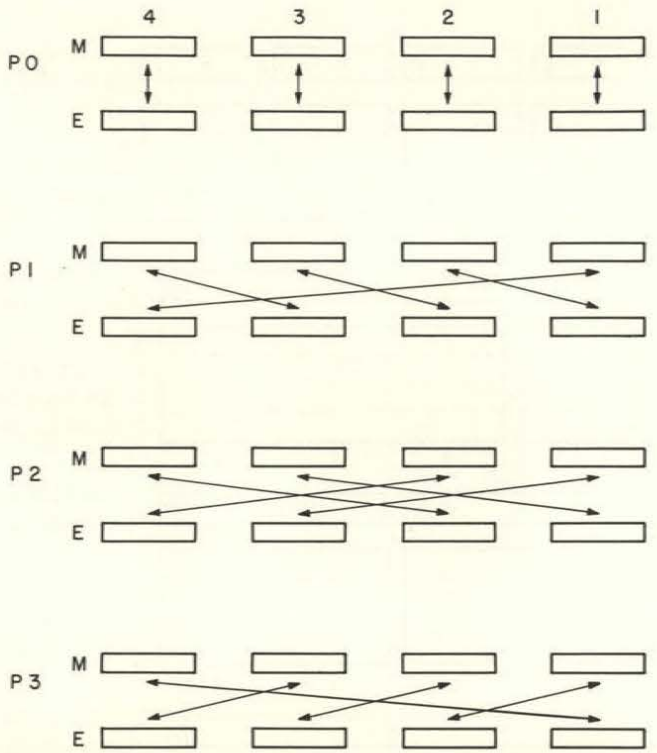

Fig. 10(b). Paths in exchange element.

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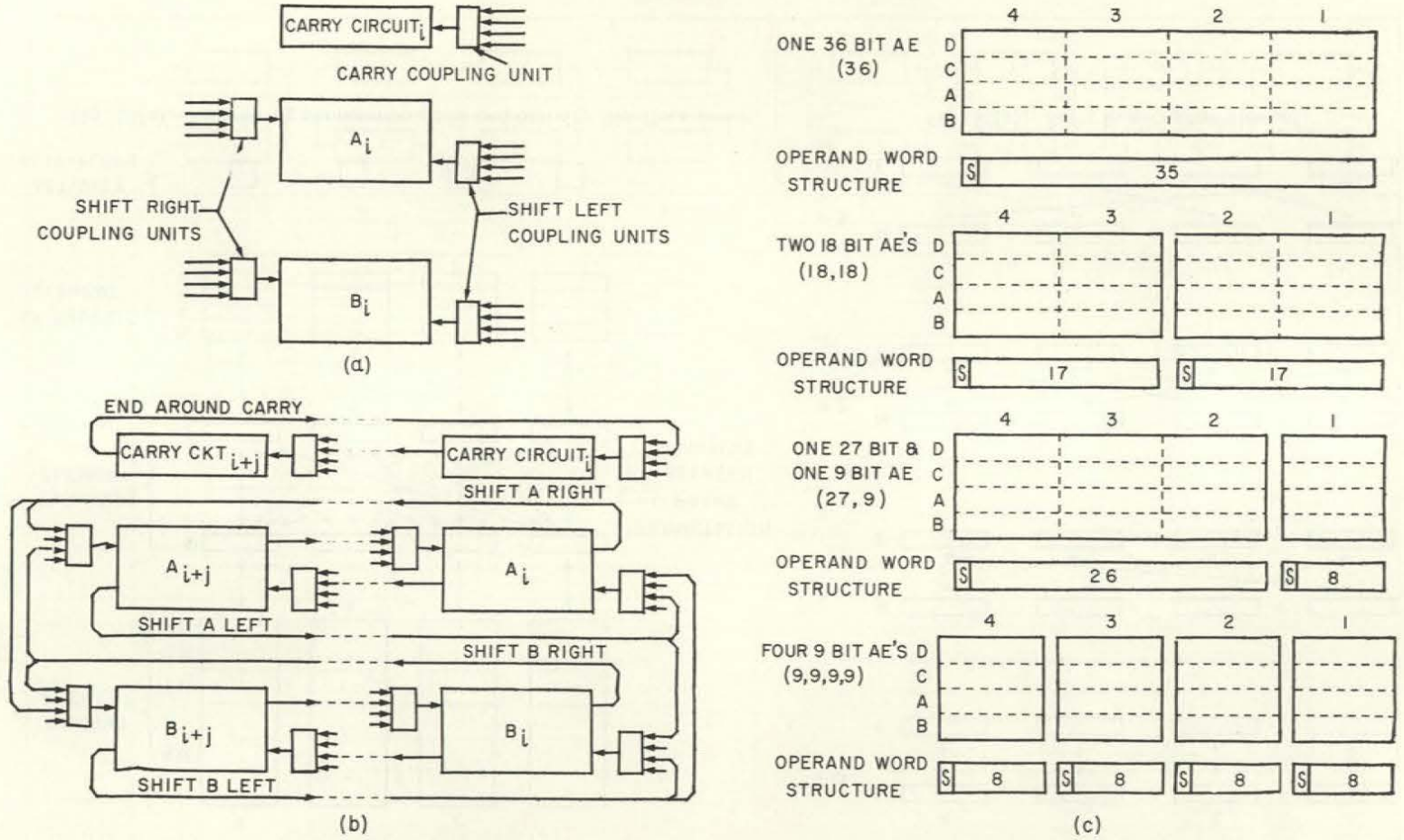

Fig. 11(a). ith quarter coupling units; (b) coupling unit connections; (c) TX-2 configuration – arithmetic elements and operand word structures.

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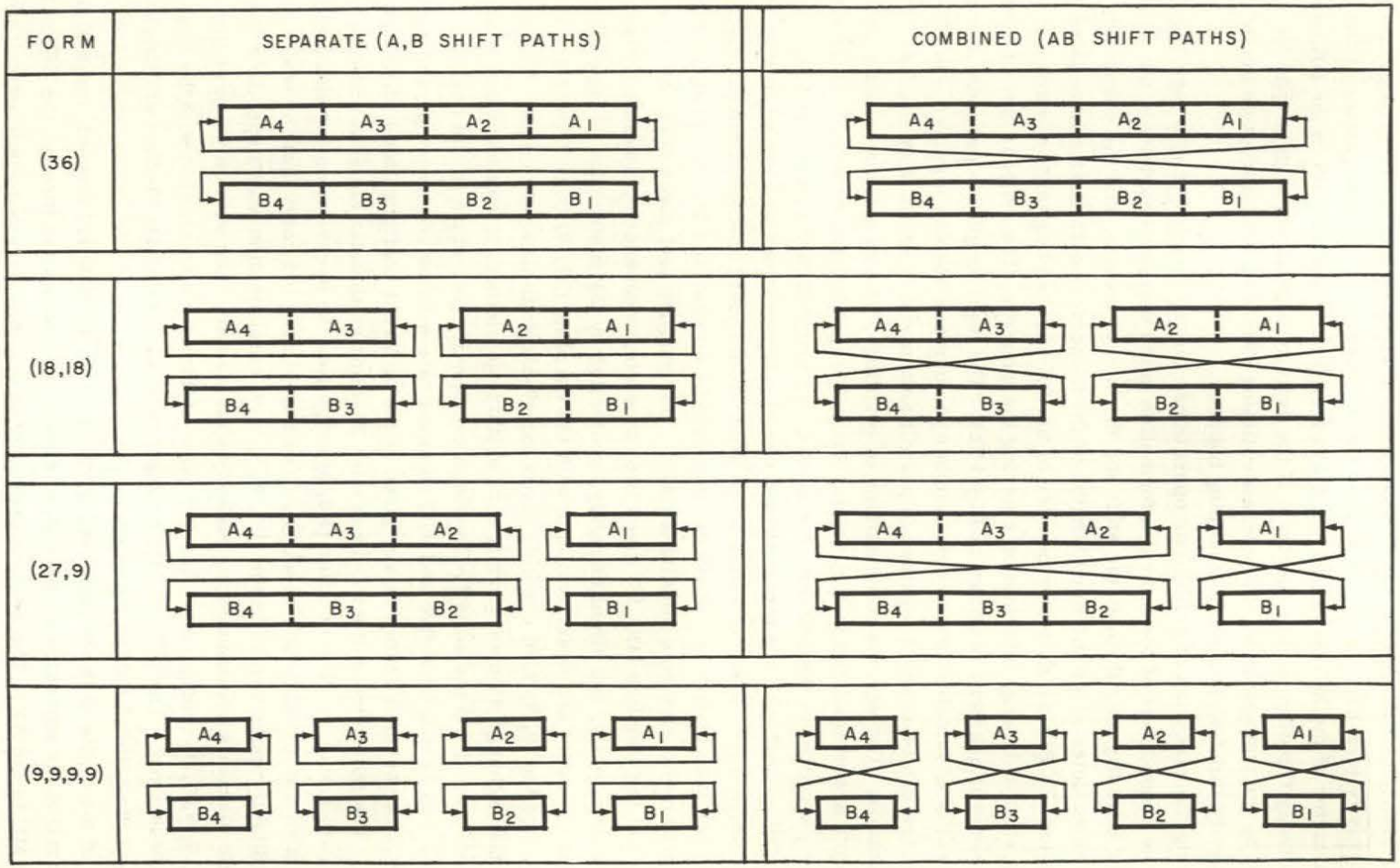

Fig. 11(d). TX-2 shift path arrangements.

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This ability to communicate is focused more sharply by having the configuration specify a system activity (see Fig. 9). All operation timing events, in a given quarter of the AE and EE and the quarter of the ME connected via the selected permutation path in the EE, are controlled by the activity flip-flop on that quarter. If the activity flip-flop of a given quarter is a ONE, as specified by the configuration, the operation timing events of the instruction occur in that quarter. If the activity flip-flop is a ZERO, nothing happens.

During the execution of arithmetic operations, the AE coupling digits (see Fig. 9) further specify the connections of the lateral information paths between quarters in the AE. Information flows laterally only through the shift and the carry circuits, and the connection of these circuits alone determines the word lengths of the numerical quantities manipulated in the AE.

As shown in Fig. 11(a), every quarter of the AE has coupling units at each end which receive the shift and carry information entering the quarter. The general type of connections between several quarters is shown in Fig. 11(b). The digit length of operands, during add and shift operations, is determined by the number of quarters coupled together. In TX-2, from 1 to 4 quarters can be coupled together to permit arithmetic operations on 9-, 18-, 27-, or 36-digit operands. The various combinations of coupling-unit connections actually chosen by the AE coupling are symbolized in Fig. 11(c). Since A-register, B-register, and AB-register shifts are permitted in the arithmetic element, the programmer can obtain 18-, 36-, 54-, or 72-digit shifts. All the possible shift (and cycle) configurations are shown in Fig. 11(d).

Only those inputs to the coupling units which would yield useful arithmetic element structures are realized by the AE coupling. It should be emphasized that the programmer can realize several arithmetic elements simultaneously. The coupling (36) gives only one 36-bit arithmetic element, but the coupling (18, 18) gives two complete, independent, 18-bit arithmetic elements which are separately, but simultaneously, controlled by the instruction being executed. Two arithmetic elements are again available with the coupling (27, 9), one 27 bits and the other 9 bits long, and the (9, 9, 9, 9) coupling gives four 9-bit arithmetic elements. The permutation paths in the exchange element permit each arithmetic element to communicate with any quarter of a memory word and the activity flip-flops can specify just which of the realized arithmetic elements actually will be active and will communicate with the connected part of memory.

In Fig. 12, several examples are given of the different configurations which can be realized in TX-2. The most straightforward has one 36-digit arithmetic element and communicates directly with memory. The notation (P0, 36) signifies the permutation (no shift) and the form of the arithmetic element (one 36-digit). The underlining indicates that the whole system is active. Slightly more varied is the (P0, 9, 9, 9, 9) configuration which specifies four 9-digit arithmetic elements communicating directly with memory, but with only two of them active. The (P2, 9, 9, 9, 9) configuration has the same arithmetic elements but with the associated memories interchanged. The (P2, 18, 18) configuration illustrates an 18-digit arithmetic element which uses the "other" half of memory.

One of the digits in the 9-digit configuration is at the moment unused, but will probably be used to control the extension of the sign of numbers as they pass through the EE on the way from the ME to the AE. The scheme presently under consideration would permit programmers,

for example, to add a 9-digit memory operand to an 18-digit arithmetic element. This scheme would permit closer packing of operands in memory and significantly increase the speed of solving some real-time problems, where the sign of short pieces of data must be extended so that higher precision can be maintained during computations. The working details of the scheme have yet to be fixed.

The memory from which the programmer chooses a configuration for use with each instruction was shown in Fig. 9. Twelve of the memory registers are fixed circuitry whose contents

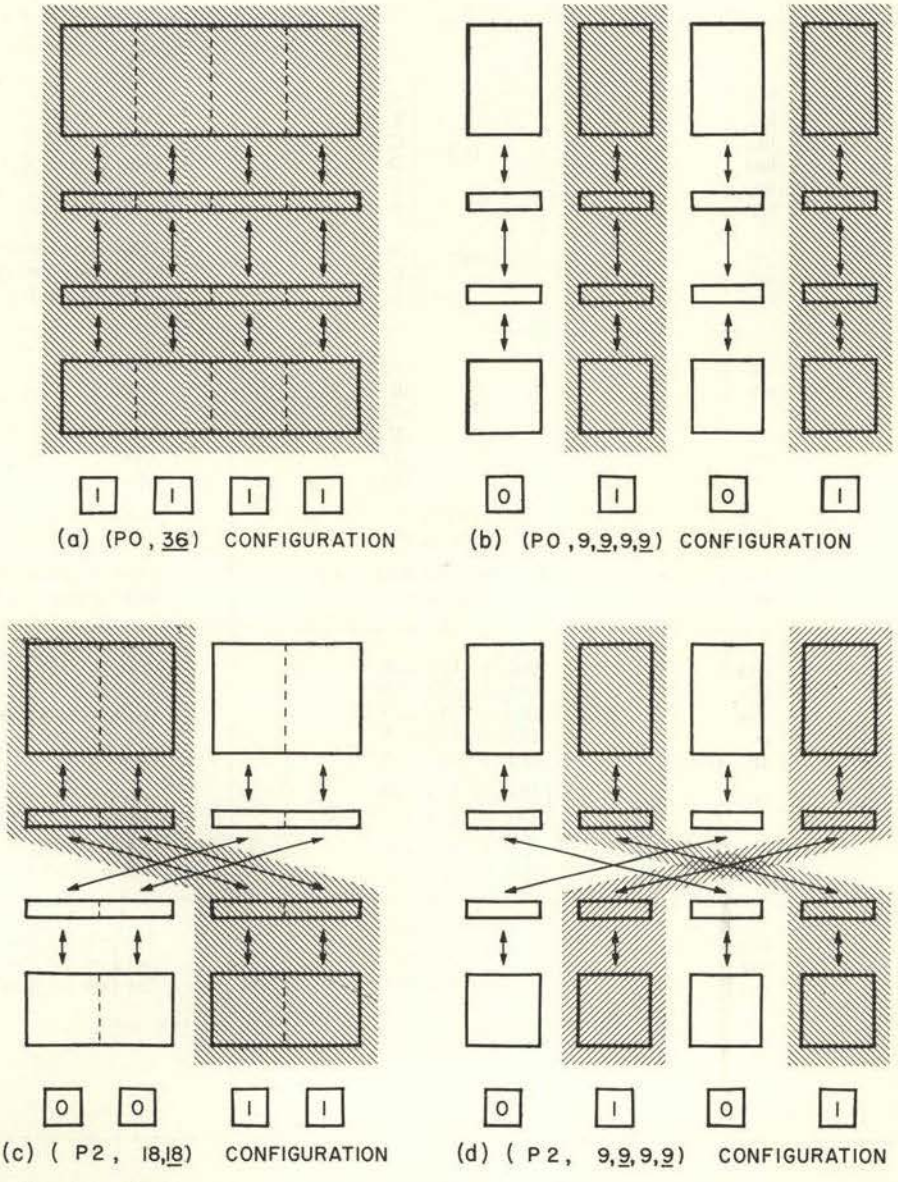

Fig. 12. TX-2 configurations. Areas of activity during execution of instruction shown shaded; effect of AE couplings illustrated by juxtaposition of quarters.

TABLE I

Type	Mnemonic Code	Operation	Name
Load	lda	$(Y) \rightarrow A$	Load into A
	ldb	$(Y) \rightarrow B$	Load into B
	ldc	$(Y) \rightarrow C$	Load into C
	ldd	$(Y) \rightarrow D$	Load into D
	lde	$(Y) \rightarrow E$	Load into E
	ldf	$(Y) \rightarrow F$	Load into F
	lca	$(\overline{Y}) \rightarrow A$	Load complement into A
	lcb	$(\overline{Y}) \rightarrow B$	Load complement into B
	ldx	$(y) \rightarrow j$	Load into index
Store	sta	$(A) \rightarrow Y$	Store A
	stb	$(B) \rightarrow Y$	Store B
	stc	$(C) \rightarrow Y$	Store C
	std	$(D) \rightarrow Y$	Store D
	ste	$(E) \rightarrow Y$	Store E
	stf	$(F) \rightarrow Y$	Store F
	exa	$(Y) \rightarrow A$; $(A) \rightarrow Y$	Exchange A
	ins	$(B) \,\&\, (A) \vee \overline{(B)} \,\&\, (Y) \rightarrow Y$	Insert digits of A
	stx	$(j) \rightarrow y$	Store index
Add	add	$(A) + (Y) \rightarrow A$	Add
	sub	$(A) + (\overline{Y}) \rightarrow A$	Subtract
	dma	$\lvert(A)\rvert + \overline{\lvert(Y)\rvert} \rightarrow A$	Difference of magnitude
	and	$(A) \,\&\, (Y) \rightarrow A$	Logical and
	ori	$(A) \vee (Y) \rightarrow A$	Logical or – inclusive
	ore	$(A) \oplus (Y) \rightarrow A$; $(A) \,\&\, (Y) \vee (C) \rightarrow C$	Logical or – exclusive (and accumulate product)
	axm	$(j) + (y) \rightarrow y$	Add index to memory
	amx	$(j) + (y) \rightarrow j$	Add memory to index
Set bit	sbo	$1 \rightarrow Y_j$	Set j-th bit one
	sbz	$0 \rightarrow Y_j$	Set j-th bit zero
	sbc	$(Y_j)^c \rightarrow Y_j$	Set j-th bit complement

TABLE I (Continued)

Type	Mnemonic Code	Operation	Name
Step-Count	mul	$(A) \times (Y) \rightarrow AB$	Multiply
	div	$(AB) \div (Y) \rightarrow \begin{cases} A \text{ (remainder)} \\ B \text{ (quotient)} \end{cases}$	Divide
	sha sab shb	$\left.\begin{matrix}(A)\\(AB)\\(B)\end{matrix}\right\} \times 2^{(Y)} \rightarrow \begin{cases} A \\ AB \\ B \end{cases}$	Shift A Shift AB together Shift B
	cya cab cyb	$\left.\begin{matrix}(A)\\(AB)\\(B)\end{matrix}\right\} \text{cyc } (Y) \rightarrow \begin{cases} A \\ AB \\ B \end{cases}$	Cycle A Cycle B together Cycle B
	nab	$\begin{cases}(AB) \times 2^{nf} \rightarrow AB \\ (Y) - nf \rightarrow D\end{cases}$	Normalize AB
	coa	$(Y) + no \rightarrow D$	Count ONES in A
In-Out	rds	$\begin{cases}(Y) \rightarrow 10 \\ (10) \rightarrow Y\end{cases}$	Read and shift
	rdn	$\begin{cases}(Y) \rightarrow 10 \\ (10) \rightarrow Y\end{cases}$	Read without shift
Jump	jpe	If $(E_j) = 1$, then $y \rightarrow P$	Jump if j-th bit of E is a one
	jpp	If any $(A) > 0$	Jump if the contents of any A is positive
	jpn	If any $(A) \leqslant 0$	Jump if the contents of any A is negative
	jpz	If any $(A) = 0$	Jump if the contents of any A is zero
	jpo	If any (A) overflowed — then $Y \rightarrow P$	Jump if the contents of any A has overflowed
	jxp	If $(j) \geqslant 0$, then $(j) - cf \rightarrow j$, $y \rightarrow P$	Jump if index positive and decrease index
	jxn	If $(j) < 0$, then $(j) + cf \rightarrow j$, $y \rightarrow P$	Jump if index negative and increase index
	jpu	$\begin{cases}\text{If } cf = 1,3, \text{ then } (P) + 1 \rightarrow j \\ \text{If } cf = 0,1, \text{ then } y \rightarrow P \\ \text{If } cf = 2,3, \text{ then } Y \rightarrow P\end{cases}$	Jump unconditionally
Misc.	ios		In-out select
	opr		Operate

cannot be changed without changing the wiring of the computer. The configurations represented by the contents of these registers are assumed to be useful to most programmers. The last four registers in the memory consist of the 36 digits of the F-register. As will be seen, the programmer can quite simply alter the contents of this register and thereby obtain any of the possible configurations. The total number of distinct possible configurations is less than 2^9.

I. OPERATION CODE

Only 51 of the 64 possible operation codes are currently decoded to define instructions. In Table I the effect of each instruction is described. If the selected configuration defines several computers, the operation takes place in all of them simultaneously and independently. The notation used in the definition of the operation is described in Table II.

TABLE II

Notation	Meaning
$\leftarrow$	goes into
(x)	contents of x
Y = y + (j)	indexed memory address
|(x)|	magnitude of (x)
$\overline{(x)}$	ONE's complement of (x)
&	logical AND operation
v	inclusive OR operation
$\oplus$	exclusive OR operation
+	ONE's complement addition
nf	number of shifts to normalize
no	number of ONES
Y_j	j-th digit of register Y

The instructions are grouped according to type. Load and store instructions transfer an operand between a selected register and memory. The load-complement instructions are variants which load the ONE's complement into the selected registers. The exchange instruction interchanges the contents of A and of the addressed memory register. The insert instruction allows any set of bits in A, as specified by the bits in B, to be stored in memory. The j-bits of the load and store instructions, which refer to the index memory, select the index register involved so that the operand address is not modified.

All of the add and step-counter instructions can also be classed as load type instructions, in so far as the operand memory cycle is concerned. The multiply instruction forms the full product in the A and B registers. Division is the inverse of multiplication, the double-length dividend in A and B being divided by the memory operand. The remainder is left in A and the quotient in B. Normalize instructions shift the contents of A and B left until the magnitude of the number in A is between one-half and one. The number of shifts to do this (the normalizing factor) is subtracted from the memory operand in D. Since more than 18 bits are required to specify all the possible shifts for the (9, 9, 9, 9) configuration, the shift and cycle instructions use a memory operand, rather than the address section of the instruction to specify the number of places to shift. The count ONES instructions adds the number of ONE's bits in A to the memory operand in D, thus providing a simple means for determining bit density in areas of storage, since the ONE's count for several words can be accumulated in D.

The two replace-add instructions, using the index memory, facilitate instruction and index modification. Both require two memory-cycle times for execution.

The two in-out read instructions transmit information between the memory and the selected in-out unit. The details of these instructions and the in-out select instruction are given in Section III.

Single bits in memory can be manipulated with the three bit-setting instructions. The bit-sensing instruction facilitates the use of single bits in memory as operands. The variety of available jump instructions simplifies the coding of logic decision functions. The two index-jump instructions permit indexed program loops to refer successively in either the forward or backward direction to operands in a data block. The unconditional-jump instruction uses the cf digits to specify whether the selected index register will be used to remember the previous contents of P. These contents are always transmitted to the E-register whenever a jump occurs.

Arithmetic overflows can be caused by addition, subtraction, and division instructions. Such overflows as do occur are remembered in overflow flip-flops in the arithmetic element. The overflow condition can be detected by a jump instruction, or by the in-out element in a manner described in Section III. If an overflow is anticipated, however, it can be shifted into the A register by executing a normalize instruction. A normalize usually shifts AB left. However, if an overflow exists, AB is shifted right one place and the overflow placed in the most significant digit position of A to the right of the sign digit. The memory operand is also increased by one in the D register, rather than decreased. This interpretation of an overflow permits floating-point operations to be programmed very simply in the arithmetic element. The in-out select and operate instructions differ from all the others in the sense that the y-digits are used to specify different operations. In-out select chooses the mode in which an in-out unit will run. The operate instruction will control individual useful commands, e.g., round-off.

J. INSTRUCTION TIMES

The average execution time for instructions depends upon whether one memory or two different, overlapped memory systems are used for instructions and operands. If one memory is used, the execution time is the sum of the instruction and operand cycle times; if two memories are used, the execution time is the longer of the two memory cycle times. It should be remembered that any instruction which involves storing an operand in memory has the normal operand memory cycle time extended by from 1.0 to 2.0 μsecs. Instructions which alter or transfer the contents of index memory registers require approximately two memory cycles, even when instruction and operand memory cycles are overlapped.

Successive step-counter instructions require a time which depends upon the length of the longest active arithmetic element. In the case of multiply, divide, and count ONE's, this time is a function of the length of the operand word only, but the shift, cycle, and normalize times depend upon the number of places actually shifted. Divide requires about 2.0 μsecs per digit and all other step-counter instructions 0.4 μsec per digit. These shift times become significant only when they exceed the one or two memory cycles already required. In the worst 36-digit case, about 75 μsec are required for division and 19 μsec for multiplication. A 72-place shift would take 32 μsec. These are the times required for these instructions when they are written in sequence. If the operand word is shorter, then these times become proportionally less, down to the minimum memory times required.

K. SUMMARY

The organization of TX-2 permits a programmer, who pays considerable attention to coding details, to receive a worthwhile reward in the form of increased efficiency of operation. The operating speed can be doubled when instruction and operands are stored in different memories. Higher speeds result from sequencing instructions so that non-AE instructions are executed concurrently with AE step-counter instructions. And the ability to choose a configuration with each instruction means not only that some instructions take less time, but also that many of them can be eliminated from a program altogether.

However, this versatility and efficiency is not accompanied by a disastrous loss in simplicity. The system organization is such that details can be easily ignored by the naive programmer, without the details having even subtly unfavorable effects. If all the digits in an instruction word are ZERO, except for the operation code and the base address, then TX-2 appears as a simple single-address computer with operand words 36-bits long and with a single, uniformly addressed, 70,000-word memory.

If the j-bits are used, then the machine is enlarged to become an indexed, single-address, computer, with operand words 36 bits long, for which the entire instruction code is meaningful. When the b and d bits are used, the programmer can control the manner in which several in-out units, running concurrently, can cause the computer to change program sequences. And by selecting various configurations, the programmer can perform more operations simultaneously with each instruction.

The different facilities for indexing, memory overlap, instruction overlap, multiple-sequencing, and configuration can be ignored or used as the programmer desires. Ignoring them would seem to permit straight-forward coding; using them actually permits much shorter and faster codes for a given function. Each facility is represented by a clear concept of what the facility permits, the only real difficulty being the number of simultaneous actions possible with each instruction. However, higher speeds and greater system capacity are obtained by shorter cycle times, increased bit storage and greater simultaneousness of events. In TX-2, all three aspects are emphasized.

III. THE LINCOLN TX-2 INPUT-OUTPUT SYSTEM

A. INTRODUCTION

The input-output system of the Lincoln TX-2 computer contains a variety of input-output devices suitable for general research and control applications. The system is designed in such a way that several input-output devices may be operated simultaneously. Since the computer is experimental in nature, and changes in the complement of input-output devices are anticipated, the modular scheme used will facilitate expansion and modification. The experimental nature of the computer also requires that the input-output system provide a maximum of flexibility in operating and programming for its input-output devices.

The input-output devices, currently scheduled for connection to TX-2, include magnetic-tape units for auxiliary storage; photoelectric paper-tape readers for program input; a high-speed printer, cathode-ray-tube displays, and Flexowriters for direct output; analog-to-digital conversion equipment; data links with other computers; and miscellaneous special-purpose equipment. This section will not be concerned with the details of these devices, but will limit itself to a discussion of the logical incorporation of them into the system.

In describing the TX-2 input-output system, occasional reference will be made to certain aspects of the design of other parts of the TX-2 as set forth in Section II.

B. THE MULTIPLE-SEQUENCE PROGRAM TECHNIQUE

Of the various organizational schemes which permit the simultaneous operation of many devices, we have chosen the "multiple-sequence program technique" for incorporation in TX-2. A multiple-sequence computer is one that has several program (instruction) counters. If the program sequences associated with these program counters are arranged to time-share the hardware of the central computer, a machine can be obtained which will behave as if it were a number of logically separate computers. We call these logical computers sequences and therefore refer to TX-2 as a multiple-sequence computer. By associating each input-output device with such a sequence, we effectively obtain an input-output computer for each device.

Since the one physical computer in which these sequences operate is capable of performing only one instruction at a time, it is necessary to interleave the sequences if they are to operate simultaneously. This interleaving process can take place aperiodically to suit the needs of and under the control of, whatever individual input-output devices are operating. The number of sequences which can operate simultaneously, and the complexity of the individual sequences, is limited by the peak and average data-handling rate of the central computer hardware.

In a multiple-sequence computer, the main body of the computation can be carried out in any sequence, but if maximum efficiency of input-output operation is to be achieved, the bulk of arithmetic operations must be confined to a few special sequences, called main sequences, which have no associated input-output devices. The input-output sequences may then be kept short, and a large number of them can be executed at once.

C. MULTIPLE-SEQUENCE OPERATION IN TX-2

In TX-2, one-half of the index-register memory has been made available for storing program counters. Thus, a total of 32 sequences may be operated in the machine. (Actually an additional sequence of special characteristics is obtained by using index register number 0 as a program counter. This special sequence will be discussed later.) Some of these sequences are associated with input-output devices. Others perform functions, such as interpreting arithmetic overflows that are called into action by conditions arising within the central computer. Finally, there are the main sequences which are intended to carry out the bulk of the arithmetic computations performed by the machine.

A priority scheme is used to determine which sequence will control the computer at a given time. If more than one sequence requires attention at the same time, control of the machine will go to the sequence having the highest priority and instructions addressed by its program counter will be executed.

Table I is a list of the sequences currently planned for inclusion in TX-2. They are listed in approximate order of priority with the highest at the top. Asterisks mark sequences which are not associated with any particular in-out device. A special sequence (number 0) has first priority and will be used to start any of the other sequences at arbitrary addresses. The next two sequences interpret alarms (under program control). These three sequences have the highest priorities, since they must be capable of interrupting the activities of other sequences. The input-output devices follow, with high-speed, free-running units carrying next highest priorities. The main sequences (we anticipate three) are at the bottom of the list. The priority of any sequence may be easily changed, but such changes are not under program control. Priorities are intended to remain fixed under normal operating conditions. The list totals about 25 sequences, leaving eight spaces for future expansion.

TABLE I

TX-2 SEQUENCE ASSIGNMENTS IN THE ORDER OF THEIR PRIORITY

* Start-over (special index register number 0 sequence)
* In-out alarms
* Arithmetic alarms (overflows, etc.)
Magnetic-tape units (several sequences)
High-speed printer
Analog-to-digital converter
Photoelectric paper-tape readers (several sequences)
Light pen (photoelectric pick-up device)
Display (several sequences)
MTC (Memory Test Computer)
TX-0
Digital-to-analog converter
Paper tape punch
Flexowriters (several sequences)
* Main sequences (three)

*The sequences have no input-output device.

Switching between sequences is under the control of both the input-output devices (generalized to include alarms, etc.) and the programmed instructions within the sequence.

Once a sequence is selected and its instructions are controlling the computer, further switching is under control of the programmed instructions. Program control of sequence switching is maintained through two bits, called the break and dismiss bits, in each instruction. The break bit governs changes to higher-priority sequences. When the break bit permits a change, and some higher-priority sequence requests attention, a change will be made. The dismiss bit indicates that the sequence has completed its operation (for the moment, at least) and that lower-priority sequences may receive attention. The interpretation of the break and dismiss bits will be discussed in more detail.

D. THE TX-2 INPUT-OUTPUT ELEMENT

The TX-2 input-output element is shown schematically in Fig. 13. It consists of a number of input-output devices, associated buffers, and a sequence selector. Each device has enough control circuitry to permit it to operate in some selected mode once it has been placed in that mode by signals from the central computer. Associated with each device is a buffer storage of appropriate size. This buffer may be large or small, to suit individual data-rate requirements, but the buffers used in TX-2 will generally be the smallest possible. For the most part, buffering for only one line of data from the device (e.g., 6 bits for a paper-tape reader) will be provided. Each input-output device is associated with one stage of the sequence selector. The sequence selector provides the control information necessary for proper interleaving of the program sequences. When it is desired to add a new input-output device to the computer, the three packages, in-out unit, buffer, and sequence-selector stage, must be provided.

As shown in Fig. 13, data is transferred between the input-output element and the central computer by way of the exchange element. Figure 13 indicates two-way paths between the E-register and all in-out buffers. Actually, most devices are either readers or recorders, but not both, and therefore require one-way paths only. Only the necessary paths are provided; the drawing simply shows the most general case.

Signals from the sequence selector connect the appropriate buffer register to the E-register to transfer data. When a sequence is selected (i.e., its program counter is supplying instruction locations), the associated buffer is connected to the E-register, and all other buffers are disconnected. A read instruction will effect a transfer of information between the buffer and the E-register. A particular buffer is thus accessible only to read instructions in the sequence associated with the buffer's in-out unit.

Figure 13 shows paths from the sequence selector to a coder which proves an output called the program-counter number. These paths are used in the process of changing sequences to be described in a later section.

Figure 13 also shows paths for mode selection in the in-out element. The use of these paths is described in the next section under 2., ios.

E. INPUT-OUTPUT INSTRUCTIONS

In addition to the break and dismiss bits on all instructions, the programmer has three computer instructions for operating the input-output system. There are two read instructions,

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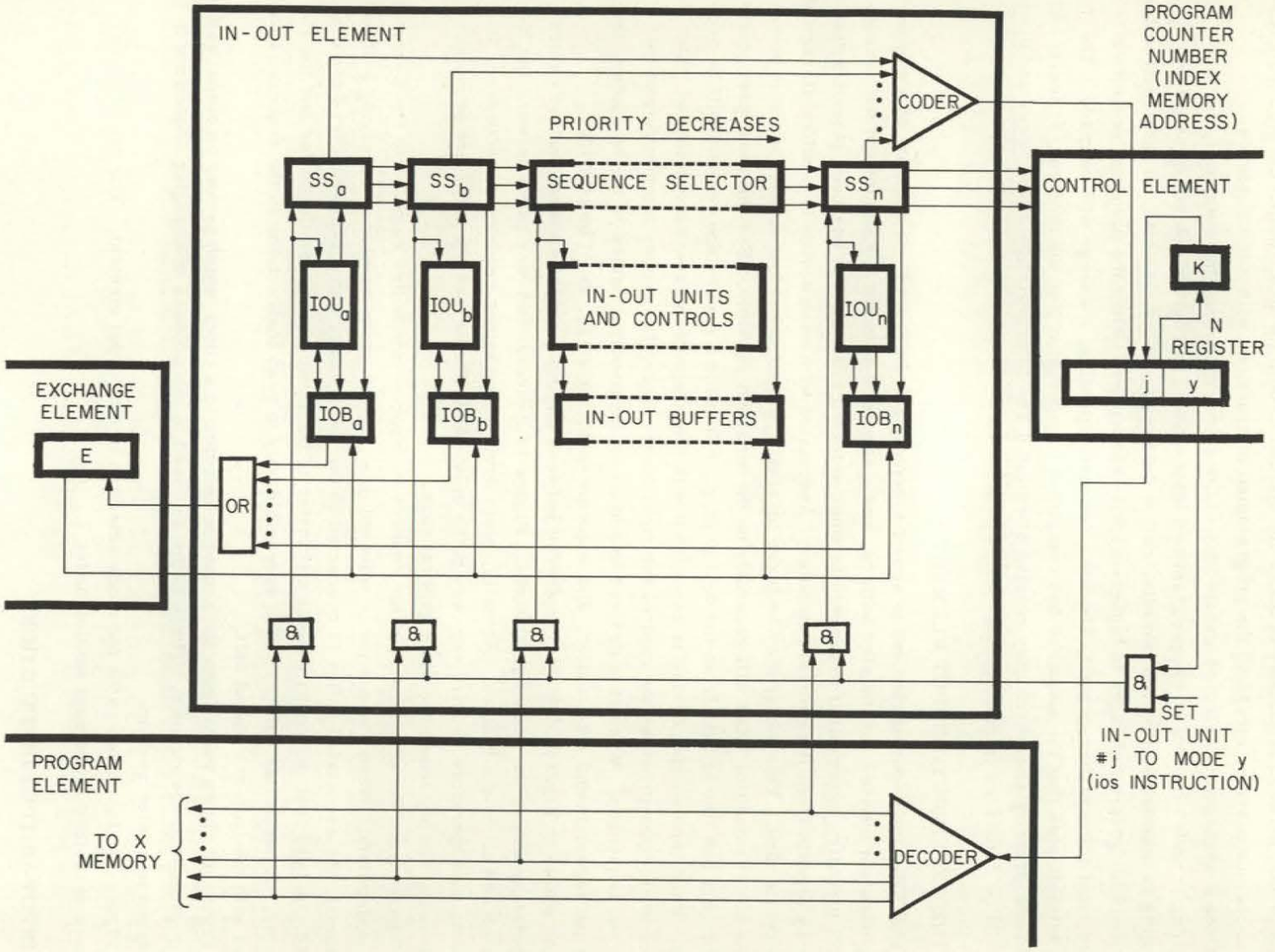

Fig. 13. TX-2 in-out element

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rdn and rds, which transfer data between the in-out devices and the central computer memory. The third instruction, ios, selects the mode of operation of the in-out devices.

1. rdn and rds

Both of the read instructions obtain a word from memory. If the in-out device associated with the sequence in which the read instruction occurs is in a reading (input) mode, appropriate bits of the memory word are altered, and the modified word is replaced in memory. If the in-out device is in a recording (output) mode, appropriate bits of the memory word are fed to the selected in-out buffer, and the word is replaced in memory. Thus, the same read instruction suffices for both input and output operations. The distinction between rdn and rds lies in the assembling of full memory words from short buffer words. An rdn instruction will place the 6 bits from a tape reader in the right 6 bits of a 36-bit memory word. The remaining 30 bits will be left unchanged. An rds instruction for the same tape reader will place the 6 bits in a splayed pattern (every sixth bit across the memory word) and will shift the entire word one place to the left before replacing it in memory. Except for the shift, the other 30 bits remain unchanged. A sequence of 6 rds instructions, one for each of 6 tape lines and all referring to the same memory address, will suffice to assemble a full 36-bit word.

The distinction between rdn and rds could be obtained from mode information in the in-out device, but the inclusion of both instructions in the order code allows the programmer to interchange the two types freely to suit his needs. The rdn instruction makes use of the permutation aspect of the TX-2 configuration control and is, therefore, particularly convenient for dealing with alphanumeric Flexowriter characters. Configuration is not applicable to the rds instruction.

2. ios

The ios instruction serves to put a particular in-out device into a desired mode of operation. The j-bits of the instruction word, normally the index register number, in this case specify the unit number of the in-out device. This number is the same as the program counter number for the associated sequence, although the correspondence is not necessary. The y-bits of the instruction word specify the mode of operation in which the unit is to be placed. Two of the y-bits are sent directly to the jth sequence selector stage and serve to control the sequence, regardless of the mode of its associated in-out device. These two bits allow ios instructions to arbitrarily dismiss or request attention for any sequence in the machine. By means of these instructions, one sequence can start or stop all others in the machine. A third y-bit determines whether the mode of the in-out device is to change as a result of the instruction. If it is to change, the remaining 15 bits specify the new mode. An ios instruction occurring in any sequence can thus start or stop any sequence and/or change the mode of its in-out device.

A further property of the ios instruction is that it leaves in the E-register a map of the state of the specified in-out control prior to any changes resulting from the instruction itself; ios instructions may, therefore, be used to sense the state of the in-out system without altering it in any way.

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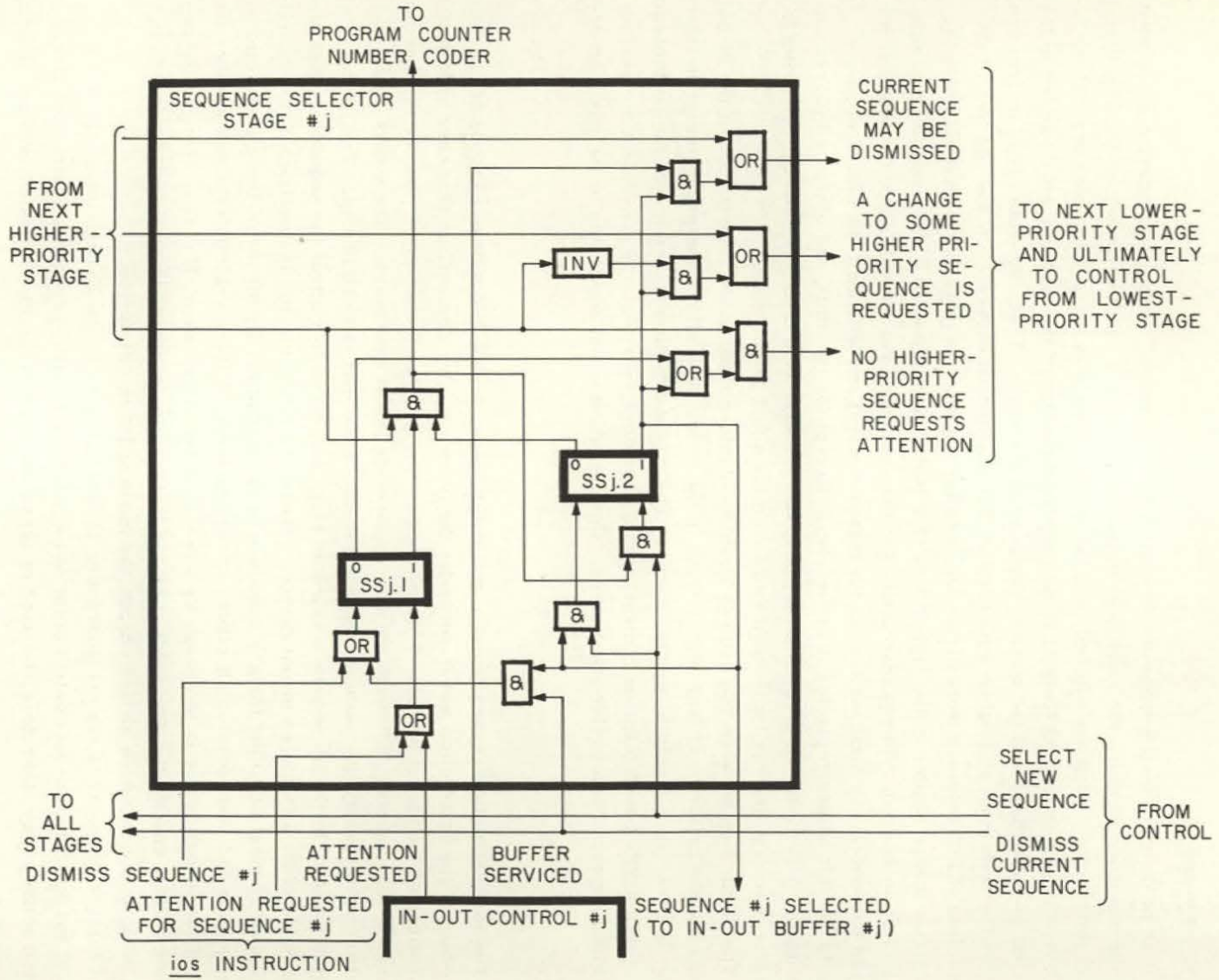

Fig. 14. TX-2 sequence selector stage

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F. SEQUENCE-CHANGING AND OPERATION OF THE SEQUENCE SELECTOR

At some point just before the completion of the instruction memory cycle in TX-2, the control must decide whether the next instruction would be taken from the current sequence or from some new sequence. The information on which this decision must be based comes from the break and dismiss bits of the instruction word currently in use and from the sequence selector. Figure 14 is a detailed drawing of one stage of the sequence selector. All stages, except that with the highest-priority are identical. The lowest-priority stage returns the final three control signals to the control element.

Each stage of the sequence selector retains two pieces of information concerning its associated sequence. One flip-flop (ss j.1) remembers whether or not the sequence is selected (i.e., whether or not it is receiving attention). The priority signal (labelled no higher priority sequence requests attention) passes from higher to lower priority stages until it encounters a stage which requests, but is not receiving, attention. Such a stage is said to have priority at the moment, and its output to the program-counter-number coder prepares the number of the new program counter in anticipation of a sequence change.

The process of changing sequences involves storing the program counter for the old sequence and obtaining the counter for the new. Actually, to speed up the over-all process, the new program counter is obtained first, so that it may be used while the old is being stored. Using the paths shown in Fig. 13, the new program counter number is placed in the j-bits of the N-register. The new program counter is then obtained from the X-memory and interchanged with the old program counter contents which have been in the P-register.* The K-register, which has been holding the old program counter number since the last sequence change, is now interchanged with the j-bits, and the old counter is stored at the proper location in the X-memory. The state of the sequence selector is changed, to conform to the change of sequence, by sending a select new sequence command from control. This command clears the ss j.2 flip-flop in the old-sequence stage and sets the ss j.2 flip-flop to a ONE in the new-sequence stage.**

G. INTERPRETATION OF THE BREAK BIT

The programmer uses the break bit of an instruction word to indicate whether or not change to a higher priority sequence may occur at the completion of the instruction. The fact that a programmer permits a break does not mean that the sequence has completed its current task, but merely that no harm will be done if a change to some higher-priority sequence is made. Breaks should be permitted at every opportunity if a number of in-out devices are operating. The sort of situation in which a break cannot be permitted occurs when the E-register is left containing information which the program requires at a later step. If a change occurred in this case, the contents of the E-register would be destroyed and lost to the program.

When a break is permitted by the current instruction, a sequence change will actually take place only if some higher-priority sequence requests attention. A signal from the sequence

*The P-register is shown in Fig.6 of Section II.

**The relative timing of the central computer actions during the change process is shown in Fig.8(d).

selector to the control element provides this information (Fig. 14). When a break type of sequence change is made, the ss j.1 flip-flop in the sequence selector remains unchanged, and the sequence which was abandoned in favor of one of a higher-priority continues to request attention.

H. INTERPRETATION OF THE DISMISS BIT

The dismiss bit is used by the programmer to indicate that the sequence presently in use has completed its task. To provide synchronization in the in-out system, dismiss bits must be programmed between attention requests from the in-out devices. In this case, the dismiss in-operation guarantees that the computer will wait for the next signal from the in-out device before proceeding with the associated program sequence.

The dismiss bit is also used to accomplish the halt function in TX-2. A multiple-sequence computer halts when all sequences have been dismissed and all in-out units turned off. The priority signal from the sequence selector to the control element provides the information as to whether or not any sequence in the machine requests attention. When none requests attention, the control stops all activity in the machine as soon as a dismiss bit appears on an instruction in the sequence being used. Activity is resumed in the machine as soon as some in-out device or push button requests attention.

The sequence change which results from a dismiss bit is identical with that resulting from a break except that a dismiss current sequence command accompanies the select new sequence command from control to the sequence selector (Fig. 14).

I. STARTING A MULTIPLE-SEQUENCE COMPUTER

In a single-sequence computer the starting process involves resetting the program counter to some arbitrary value and starting the control. In a multiple-sequence computer, the program counter for a particular sequence must be reset and the sequence started. In TX-2 a special sequence (number 0) has the highest priority and is used to facilitate starting. This sequence has the special feature that its program counter always starts at an initial memory location specified by a set of toggle switches. Attention for the sequence is requested by pushing a button on the console. By executing a short program stored in the toggle-switch registers of the V-memory, this sequence can start (or stop) any other sequence in the machine. The starting process for an arbitrary sequence involves resetting its program counter by means of an ldx (load index register) instruction, and starting its sequence with an ios instruction.

J. THE ARITHMETIC ELEMENT IN MULTIPLE-SEQUENCE OPERATION

While efficient operation requires that the bulk of arithmetic operations be carried out in a main sequence, the arithmetic element in TX-2 is available to all sequences. Since once a change has been made to a higher-priority sequence, control cannot return to a lower-priority sequence until the higher-priority one has been dismissed, a simple rule allows the arithmetic element to be used in any sequence without confusion. If, whenever a higher-priority sequence requires the arithmetic element, it stores the contents of any registers it will need (A, B, C, D or F) and reloads them before dismissing, all lower-priority sequences will find the registers as they left them. This storing and loading operation requires time and, therefore, lowers the

total handling capacity, but the flexibility obtained may well be worth the loss in capacity.

The step-counter class of arithmetic element instructions is a special problem. These instructions can require many microseconds to complete, and while TX-2 is designed to allow in-out and program element instructions to take place while the arithmetic element is busy, the case can arise in which an arithmetic element instruction (load, store, etc.) appears before the AE is finished with a step-counter class instruction. The machine would normally wait in an inactive stage until the operation is complete, but since there is a chance that some higher-priority sequence may request attention in the interim and have instructions which can be carried out, provision is made to keep trying changes to higher-priority sequences as they request attention. The machine thus waits in an inactive state only when no higher-priority sequences have instructions which can be performed. This provision allows the programmer to ignore the arithmetic element in considerations of peak- and average-peak rate calculations when he desires to operate a maximum number of in-out devices.

K. CONCLUSIONS

Multiple-sequence operation of input-output devices, as realized in TX-2, has a number of significant characteristics. Among them are:

1. A number of in-out devices may be operated concurrently with a minimum of buffering storage.
2. Machine time is used efficiently, since no time need be lost waiting for input-output devices to complete their operation. Other machine activity may proceed meanwhile.
3. Each input-output device may be treated separately for programming purposes. Efficiency of operation is obtained automatically when several separately programmed devices are operated simultaneously, although average- and peak-rate limitations must be considered.
4. Maximum flexibility in programming for input-output devices is obtained. The full power of the central machine may be used by each input-output sequence if desired. Routines for each device may be as long or as short as the particular situation requires.
5. The modular organization of the input-output equipment simplifies additions and modifications to the complement of in-out devices.
6. The organization of buffering storage allows the amount and kind of such storage to be tailored to the needs of the individual devices and the data-handling requirements to be met by the system.
7. The multiple-sequence program technique appears to be particularly well suited to the operation of a large number of relatively slow input-output devices of varying characteristics, as opposed to a smaller number of high-speed devices.

IV. MEMORY UNITS IN THE LINCOLN TX-2

A. INTRODUCTION

The three high-speed memories in TX-2 are random access and use ferrite cores. The largest has 65,536 words, 37 digits long, and operates at a cycle time of 6.5 μsec; it is referred to as the S-memory. The T-memory is driven entirely by transistors and has a capacity of 4096 37-digit words with a 5.5-μsec cycle time. The smallest and fastest is the X-memory which has a capacity of 64 19-digit words; its external word-selection and two cores per bit make possible an access time of 0.8 μsec and a cycle time of 4.0 μsec.

B. S-MEMORY (65,536 WORDS)

The S-memory (Fig. 15) is a coincident-current, magnetic-core unit with a storage capacity of 65,536 37-bit words. The bits in the word are read out in parallel, with a cycle time of 6.5 μsec and an access time of 2.8 μsec. (Cycle time is the time between successive strobe pulses, and access time is the minimum delay between setting the address register and strobing.) The block diagram (Fig. 16) shows that two 256-position magnetic-core switches are used to supply the READ and WRITE current pulses to the X and Y selection lines. The operating characteristics of these switches are such that the contents of the address register are no longer needed after the READ half of the cycle, and the interval between READ and WRITE may be extended several μsec under computer control to permit the other operations to occur. Two coordinates are used to select a register during READ and three coordinates are used for WRITE.

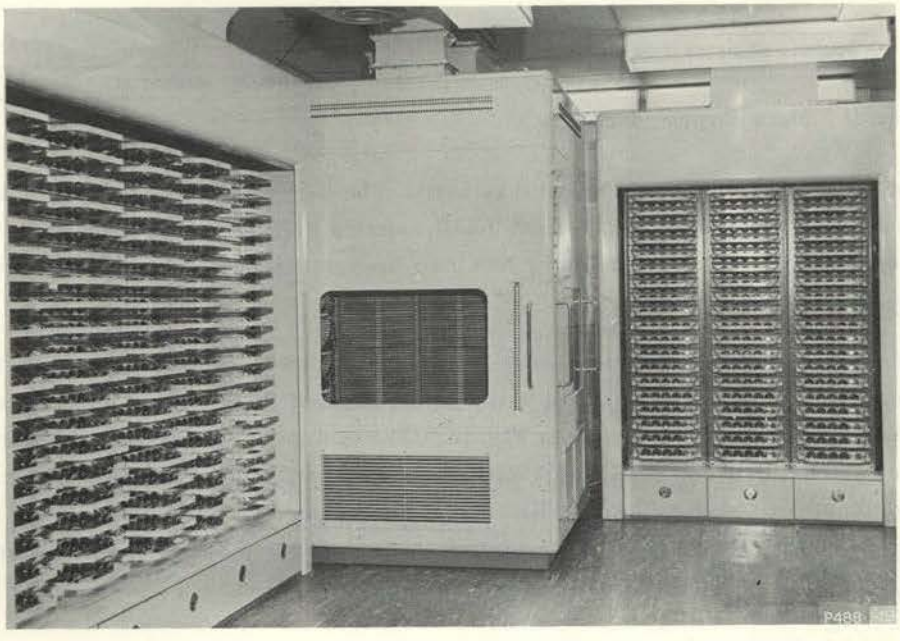

Fig. 15. S-memory.

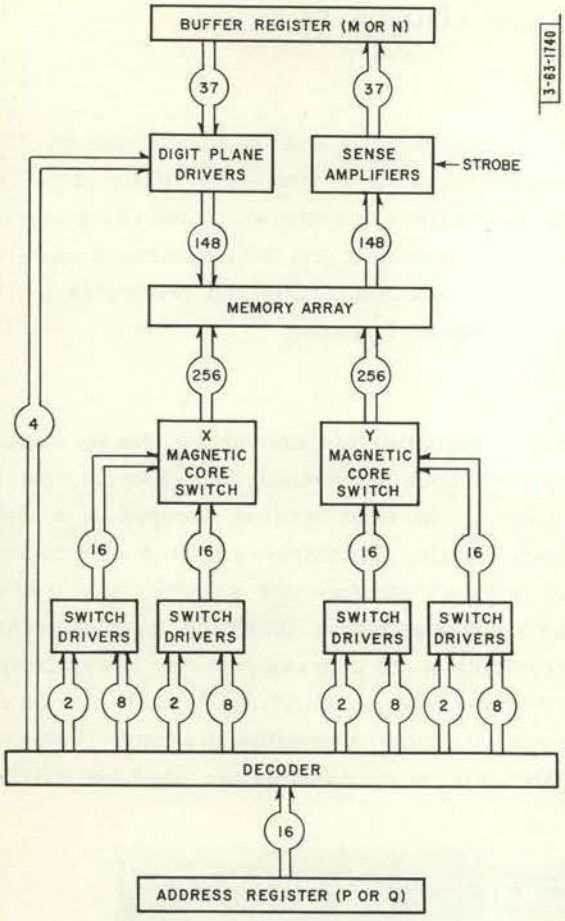

Fig. 16. Block diagram, S-memory.

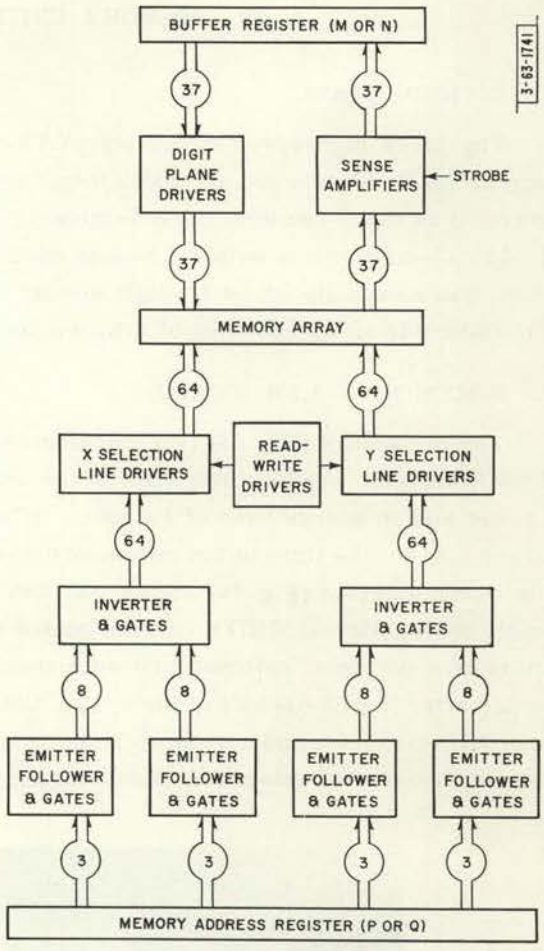

Fig. 17. Block diagram, T-memory.

In each case, a 2:1 current-selection ratio is used. The S-memory with 604 tubes and 1406 transistors is a 37-digit version of the 19-digit TX-0 memory that has been described in the literature. The basic operation of this type memory has also been described and will not be repeated here.

C. T-MEMORY (4096 WORDS)

The coincident-current, magnetic-core T-memory has 4096 37-bit words (see Fig. 17). The bits of the word are read out in parallel with a cycle time of 5.5 μsec and an access time of 2.4 μsec. A timing diagram is shown in Fig. 18. The computer program can extend, by any amount, the interval between READ and WRITE. Again, a 2:1 current-selection ratio is used with two coordinates used to select for READ and three coordinates for WRITE. A total of 1460 transistors and 64 diodes are used (not counting the address and buffer registers and control).

1. Mechanical Features

The 64 × 64 × 37 pluggable array (Fig. 19) is contained within a 5-inch cube. (One plane is used for parity checking.) The ferrite cores are 47 mils OD, 27 mils ID, and 12 mils thick. The material is similar to General Ceramics' S-1 and that is also used in the S-memory.

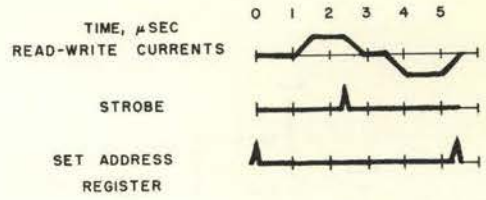

Fig. 18. Timing, T-memory.

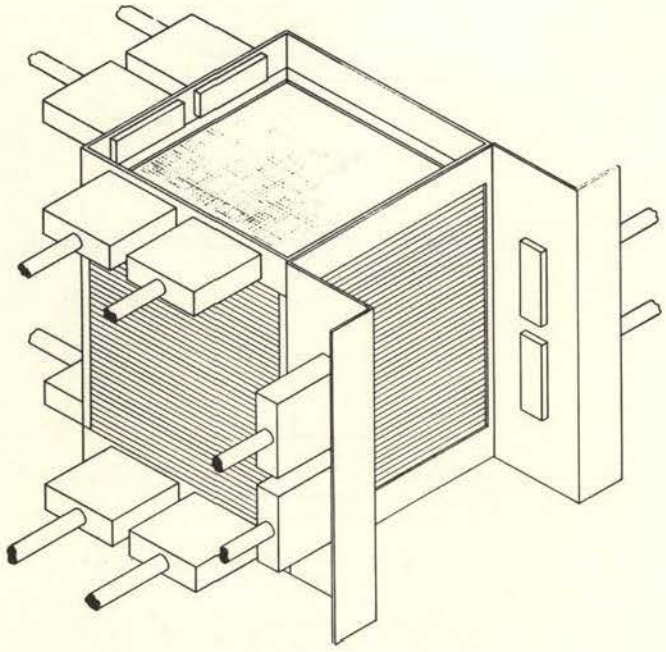

Fig. 19. Pluggable array, T-memory.

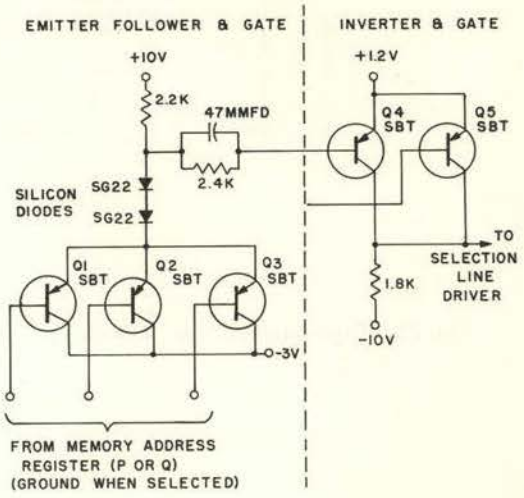

Fig. 20. One channel, emitter follower and inverter AND gates, T-memory.

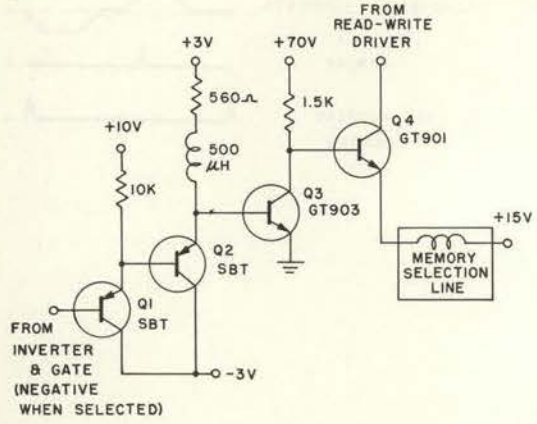

Fig. 21. One channel, selection line driver, T-memory.

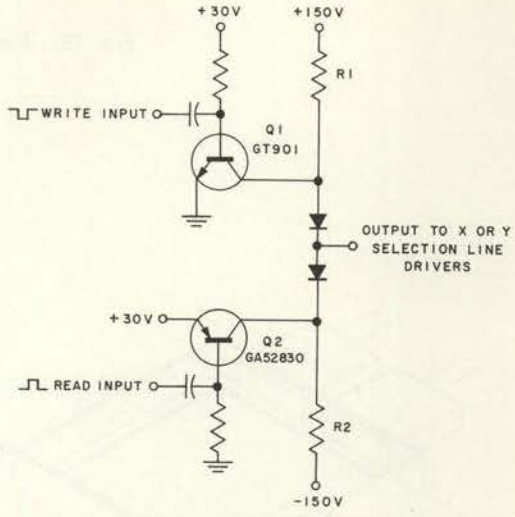

Fig. 22. READ-WRITE driver (2 needed), T-memory.

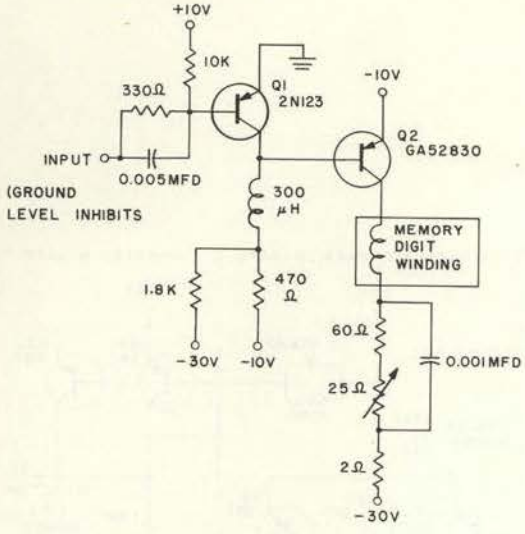

Fig. 23. Digit-plane driver, T-memory.

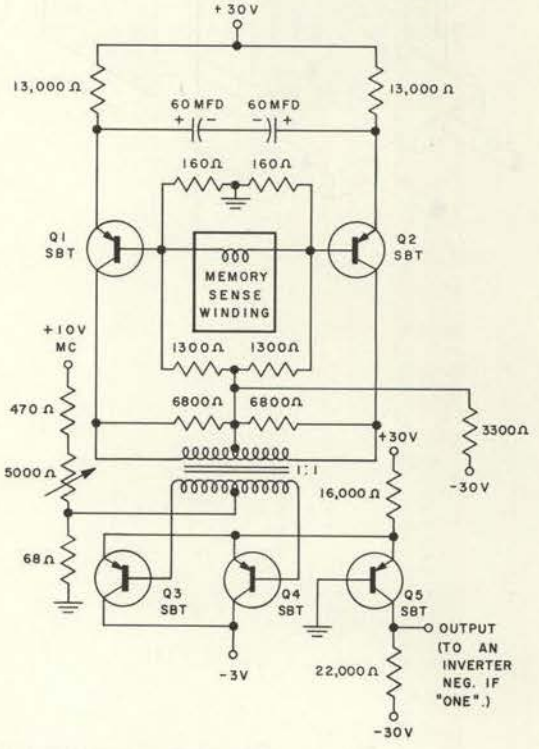

Fig. 24. Sense amplifier, T-memory.

2. Selection Circuits

The logic and circuitry of the memory-address register decoder is shown in Figs. 17 and 20. The input to the emitter follower AND gates is a d-c level of zero or −3 volts. Silicon diodes add a bias shift without the loss that would be associated with a simple voltage divider. The +1.2-volt supply for the inverter AND gates is a single divider for the whole memory – the load on the divider is constant.

Each inverter AND gate feeds a selection line driver (Fig. 21). Q4 passes the full selection line current (+250 and −250 ma) and is selected to have a minimum β of 10 for current of either polarity. The transient back voltage of the selection line for this current is 12 volts. The series-connected emitter followers (Q1 and Q2) supply the large amount of current needed to cut off Q3 quickly during selection. The load for Q2 is such that a large surge of current is delivered to Q3 to turn it on quickly when this line is deselected.

Figure 22 shows the circuit geometry planned for the read-write driver. Currents for READ and WRITE operations are supplied by the 150-volt supplies through R2 and R1, respectively. The currents are switched into the proper selection line drivers by cutting off Q1 or Q2.

3. Digit Circuits

The input of the digit-plane driver shown in Fig. 23 is a standard logic level of 0 or −3 volts. Q2 acts as a switch which connects a voltage source across the digit winding and the parallel R-C combination. It can be turned on and off very quickly by virtue of the large overdrive of current into its base which is supplied by the combination of Q1 and its collector load. The adjustable resistor is used to set the correct d-c inhibit current which is measured across the 2-ohm resistor; the 0.001-mfd capacitor speeds the current rise time in the digit winding.

In the sense amplifier, shown in Fig. 24, two 160-ohm resistors terminate the sense winding and tie it down to ground. Constant d-c emitter currents are supplied to Q1 and Q2 by the 13K resistors. The voltage divider forms a stable, d-c, collector-to-base voltage and is composed of 1.3K resistors, which form a virtual center tap on the sense-winding by operating in conjunction with the 3.3K resistor. Thus, with both the d-c emitter current and the base-to-collector voltage stabilized, the operating point of Q1 and Q2 is also stabilized. Two 60-μfd electrolytic capacitors in series tie the emitters of Q1 and Q2 together for signal gain. The 6.8K resistors damp the transformer windings. There is no gain for a common-mode input, and a gain of about 22 for a difference-signal input (output measured across half the transformer secondary). The current through the 16K resistor normally flows through Q5, but can be interrupted by an input signal that is large enough to overcome the bias on the 68-ohm resistor. The 5K variable resistance is adjusted so that a 50-mv input signal will be just enough. The normal ONE input signal is 100 mv. All of the +10-volt, marginal-check lines are tied together so that the sense-amplifier clip levels may be remotely checked to determine the memory margins.

D. X-MEMORY (64 WORDS)

There are three modes of operation of the X-memory: (1) READ-WRITE, (2) READ, and (3) CLEAR-WRITE. This magnetic-core memory requires external word-selection (two cores per bit) and has a storage capacity of 64 19-bit words. The bits of the word are read out in

parallel with a cycle time of 4.0 μsec and an access time of 0.8 μsec. In this memory, cycle time is the time between successive strobe pulses with a repetitive READ-WRITE cycle; access time is, again, the minimum delay between setting the address register and strobing. A total of 434 transistors, 8 diodes, and 1 vacuum tube are used, excluding those for the address and buffer registers and control.

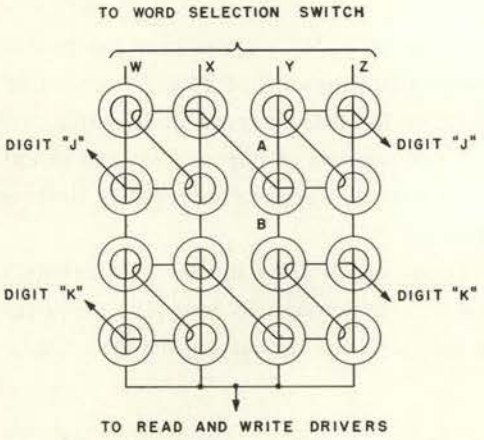

Fig. 25. Winding configuration, X-memory.

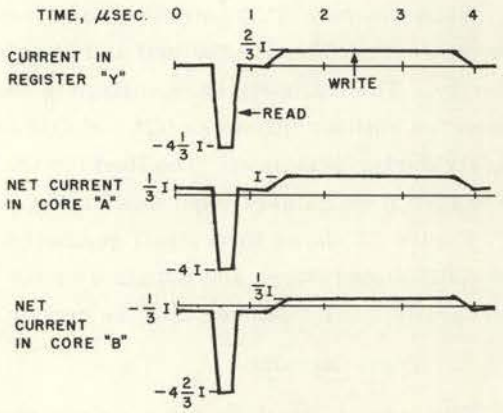

Fig. 26. Timing diagram, X-memory.

1. Operating Principle

The winding configuration of the single-plane unit is shown in Fig. 25. A word is selected externally by connecting the upper end of a word line (pt. Y, for instance) to a fixed point. The READ driver then puts out a current pulse 4-1/3 times that required to switch a core on a 2:1 basis (Fig. 26). Only one of the two cores (per bit) is switched to the cleared state by this pulse because any previous WRITE operation would have left one core set and one cleared. The switched core generates a pulse in its digit line. This line passes through one of the cores in the same direction as the word line and through the other core in a direction opposite to that of the word line. Thus, the polarity of the pulse on the digit line during READ indicates whether a ONE or a ZERO is being read out.

Current always flows in the digit winding. The polarity is controlled by the flip-flop associated with that digit, and the amplitude is 1/3 of the required switch current in a 2:1 system. The digit current is swamped out by the large read current and, therefore, has no effect during READ. During WRITE, a current of 2/3 is sent down the selected word line. The digit current adds to the write current in one core and subtracts from it in the other, so that one core has a current of unity and the other a current of 1/3. Thus, the current ratio used during WRITE is 3:1 with a disturb current of no more than 1/3. Figure 26 shows the timing and current relationships in cores A and B of Fig. 25.

The cores used for the X-memory are 47 mils OD, 27 mils ID, and 12 mils thick. The core material is similar to General Ceramics' type S-3 which differs from S-1 in that the coercive force required for switching is lower and the switching time is longer. We needed the low coercive force so that we could drive the cores with transistors. Access time remained short

because, even with transistors, we could overdrive the cores during READ. Each winding makes four turns on each core through which it passes. Figure 27 shows the complete memory plane (4-1/4 × 6-1/4 inches), and Fig. 28 shows part of it enlarged. The cores are mounted on a lucite plate; the wires pass through openings made by the intersection of milled slots on one side of the plate with similar slots on the other side that are milled at right angles to the first. With each winding making four turns per core, the digit current is 8 ma, the write-driver output current is 18 ma, and the read-driver current is 117 ma.

A block diagram of the X-memory is shown in Fig. 29. The method of word selection used is determined partially by the computer's use of the outputs of the j-bits decoder. Either of two write drivers is used and the output of the first level selection determines which one.

2. Selection Circuits

One channel of the selection circuit is shown in Fig. 30. The j-bits decoder uses 5-way emitter follower AND gates which drive parallel inverters (Q6 and Q7). The collector lead of these transistors provides an overdrive of base current into Q8 or Q9 during both selection and de-selection. When neither the read nor the write driver is active, the word lines are free to float between 0 and −10 volts. Only one of the first level selection transistors (Q10 or Q11) will be saturated, so base current flows only into either Q8 or Q9. The read driver generates a negative pulse so that the large read current (117 ma) flows in the normal direction through the 2N123's. The write current flows in the reverse direction, but it is only 18 ma, and does not require a very high reverse β. A decoder such as that in the T-memory would have used fewer transistors, but access time is at a premium here, so the faster circuit was used.

3. Read-Write Drivers

The read driver shown in Fig. 31 consists of three SBT transistors in series (because of the voltage needed) driving a 6197 pentode to saturation. The back voltage presented by the cores to this driver is constant because, as mentioned before, it always switches one of the two cores in each pair. The 5:1 transformer holds the tube load to a low value.

The write driver (Fig. 32) is very simple. The current in the 1640-ohm resistor is switched into the memory load during WRITE by saturating Q2 which cuts off Q1. Since the selection circuits are returned to −3 volts, the output terminal of this circuit is always below ground.

4. Digit Circuits

The digit driver (Fig. 33) is connected directly to the corresponding flip-flop in the buffer X-register. One of the two transistors is always saturated so that current always flows in the digit winding and in a direction determined by the flip-flop. The terminals of the digit winding are connected to the input stage (Q1 and Q2) of the sense amplifier shown in Fig. 34 which responds to the voltage difference between the inputs. The open-circuit READ signal on the digit winding is a 0.25-μsec pulse ±0.5 volt amplitude. The sense amplifier loads the winding to reduce the pulse to about half of this amplitude. A saturation signal is fed to the gates Q3 and Q5 so that the strobe pulse forces the flip-flop to the correct position. If the signal on the free end of the digit winding is positive, the flip-flop is left in the same state; if negative, the flip-flop is complemented.

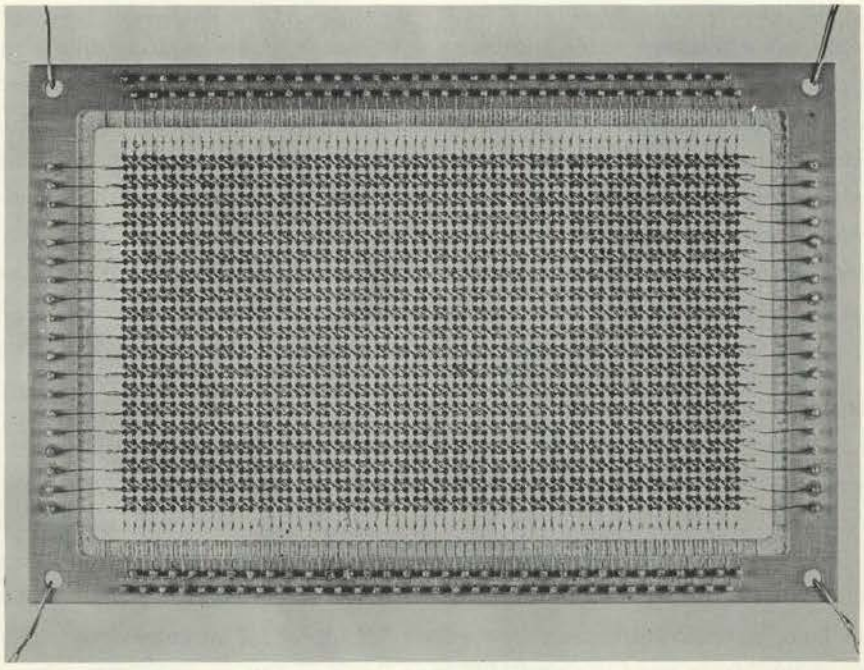

Fig. 27. 64 × 38 memory plane, X-memory.

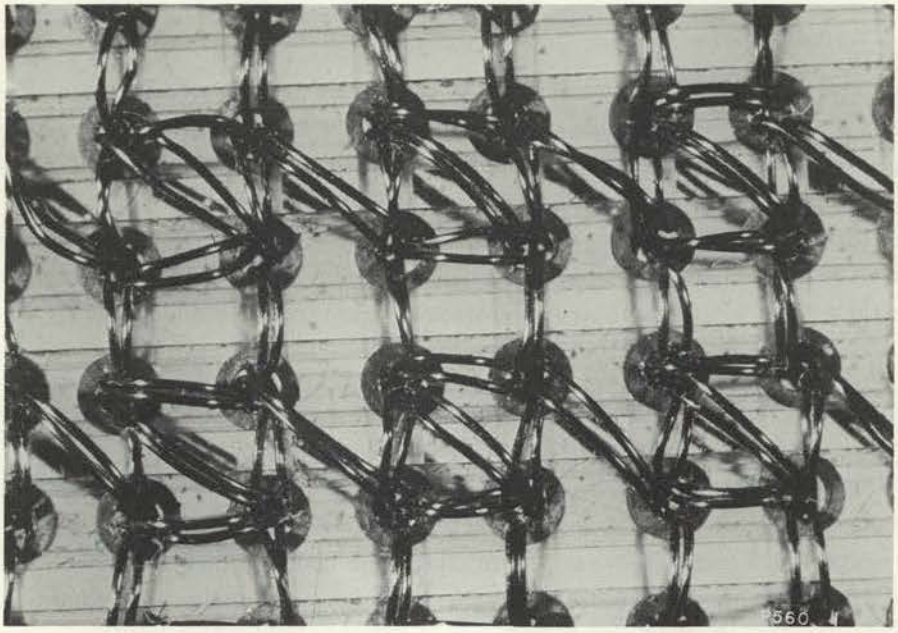

Fig. 28. Section of memory plane, enlarged, X-memory.

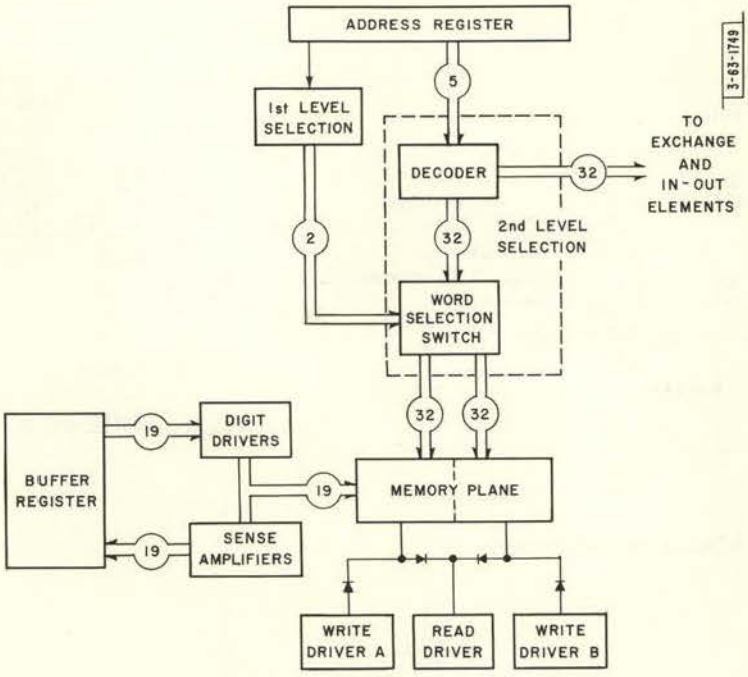

Fig. 29. Block diagram, X-memory.

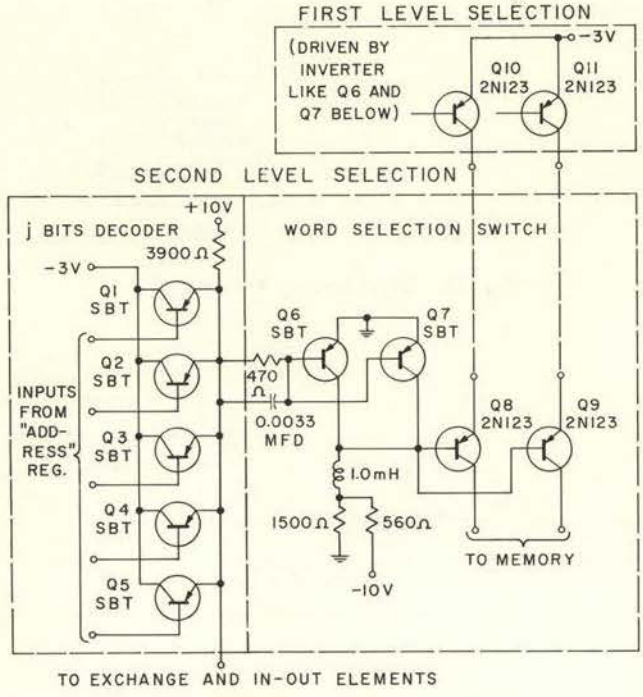

Fig. 30. Register selection circuit, X-memory.

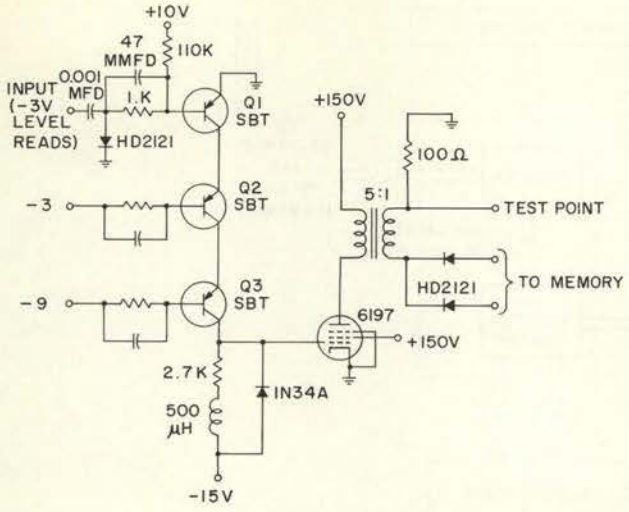

Fig. 31. READ driver, X-memory.

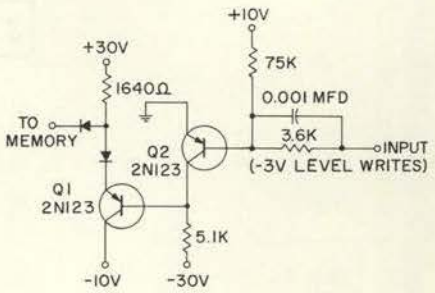

Fig. 32. WRITE driver, X-memory.

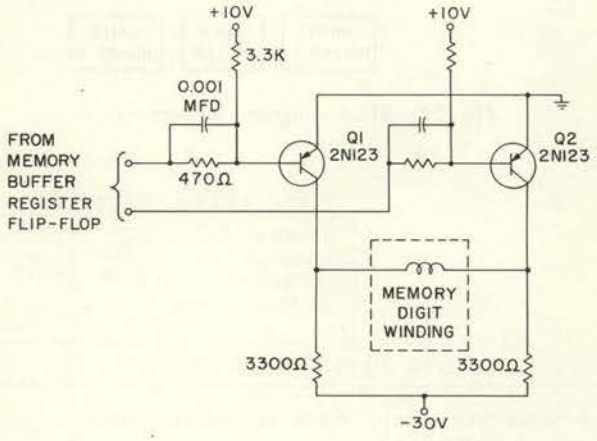

Fig. 33. Digit driver, X-memory.

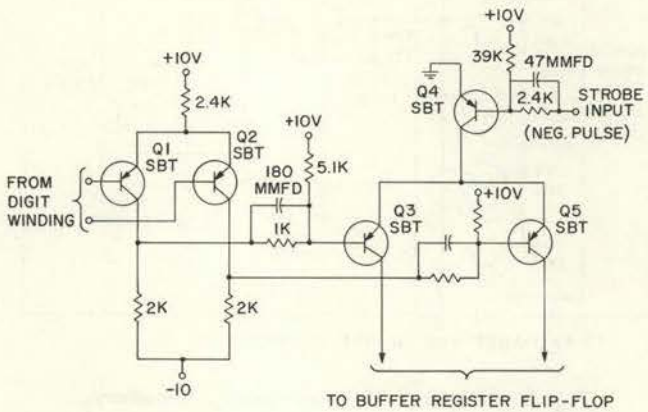

Fig. 34. Sense amplifier, X-memory.

5. Modes of Operation

The three modes of operation of the X-memory are READ-WRITE, READ, and CLEAR-WRITE. READ-WRITE has been described above. The READ operation, used when the contents of two registers are needed quickly, performs the necessary function of clearing both cores in each bit before writing. When the computer returns to WRITE in registers that have had a READ cycle only, the CLEAR-WRITE cycle is used. CLEAR-WRITE is the same as READ-WRITE except that the strobe pulse is eliminated. Actually, a WRITE cycle alone would be sufficient but the CLEAR-WRITE cycle was added as an aid to program trouble-shooting, since if a WRITE operation should follow a previous WRITE operation on the same register, some bits would have both cores set. A subsequent READ would clear both cores, their outputs would subtract in the digit winding, and the response of the sense amplifier would be unpredictable.

E. ACKNOWLEDGMENT

The achievements reported above were the result of the imagineering of many people associated with core memory development at Lincoln Laboratory. Major contributions to the system and circuit design were made by S. Bradspies, G. A. Davidson, D. H. Ellis, and J. L. Mitchell. E. A. Guditz was responsible for most of the ideas incorporated in the mechanical design and packaging.

V. TX-2 CIRCUITRY

A. CIRCUIT CONFIGURATIONS

Two basic circuits perform most of the logical operations in the TX-2 computer: a saturated transistor-inverter and a saturated emitter-follower. To the logic designer who works with them, these circuits can be considered as simple switches which are either open or closed.

The schematic diagram of an emitter follower and the symbol used by the logic designers is shown in Fig. 35. With a negative input, the output is "shorted" to the –3 volt supply, as through a switch. When several of these emitter followers are combined in parallel, as in Fig. 36, any one of them will clamp the output to –3v. We have then an OR circuit for negative signals and an AND circuit for positive signals. The transistor inverter is shown in Fig. 37 with its logic symbol. Basic AND and OR circuits result from the connection of these simple switches in series or parallel, as in Figs. 38 and 39. More complex networks like the TX-2 carry circuit use these elements arranged in series-parallel as shown in Fig. 40.

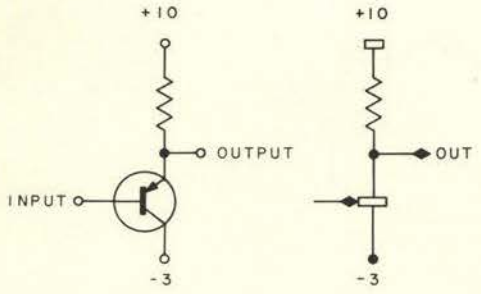

Fig. 35. Emitter follower.

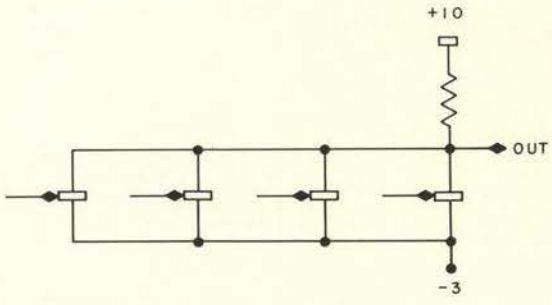

Fig. 36. Parallel emitter follower.

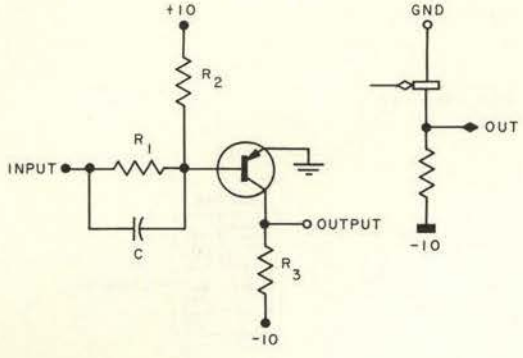

Fig. 37. Inverter.

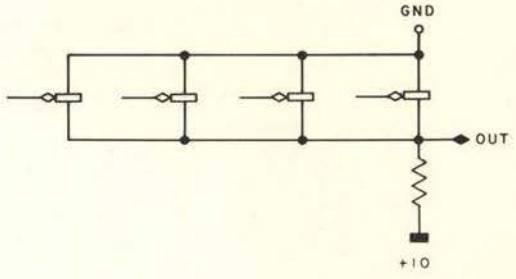

Fig. 38. Parallel inverters.

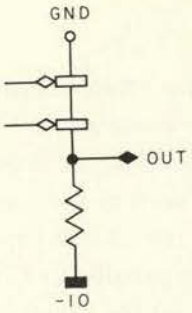

Fig. 39. Series inverters.

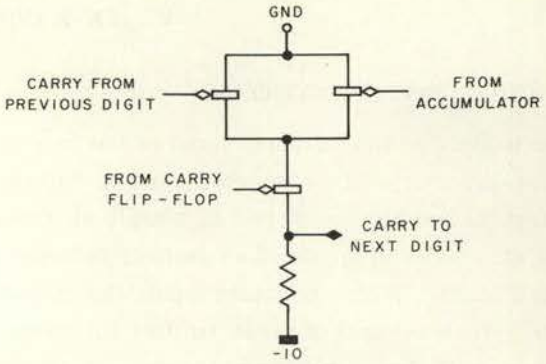

Fig. 40. TX-2 carry circuits.

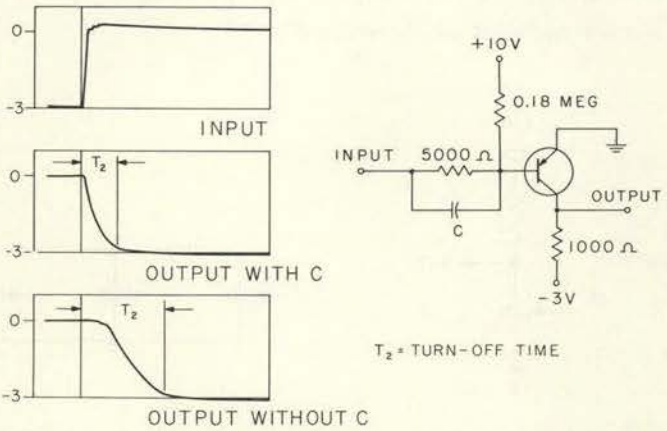

Fig. 41. Turn-off time.

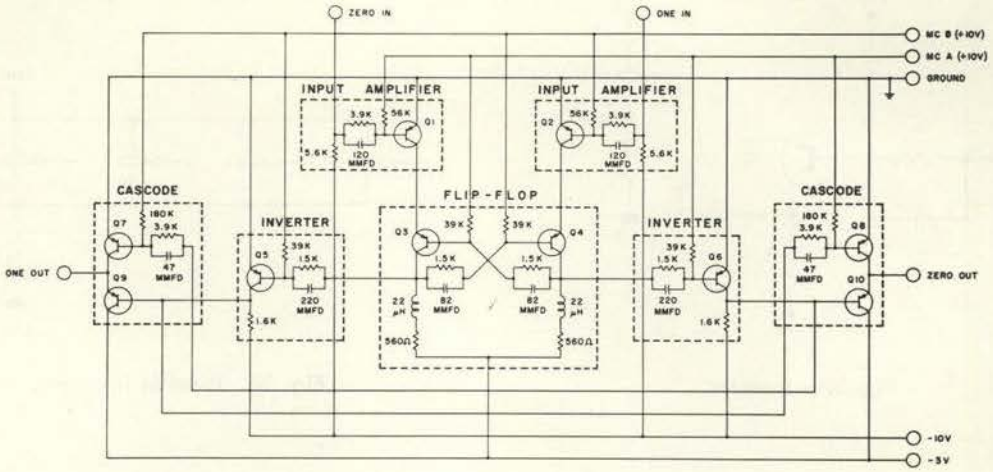

Fig. 42. TX-2 flip-flop.

In Fig.37 the resistor, R_1, is chosen so that under the worst combinations of stated component and power supply variations, the drop across the transistor will be less than 200 mv during the "on condition." R_2 biases the transistor base positive during the off condition to provide greater tolerance to noise, I_{co}, and signal variations. Capacitance, C, was selected to remove all of the minority carriers from the base when the transistor is being turned off. The effect of C on a test circuit driven by a fast step is shown in Fig. 41. Note that the delay due to hole storage is only a few millimicroseconds.

We run the circuits under saturated conditions to achieve stability and a wide tolerance to parameters without the need for clamp diodes. Unlike vacuum tubes, which always need an appreciable voltage across them for operation, a transistor requires practically no voltage across it. In spite of the delay in turning off saturated transistors, these circuits are faster than most vacuum-tube circuits. Faster circuit speed is not due to the fact that the transistors are faster than vacuum tubes, but because they operate at much lower voltage levels. A vacuum tube takes a signal of several volts to turn it from fully "on" to fully "off"; a transistor takes less than one volt.

B. FLIP-FLOP

On the basis of previous experience, we decided that the advantages of having one standard flip-flop were worth some complication in TX-2 circuitry. The circuit diagram of the flip-flop package in Fig. 42 is basically an Eccles-Jordan trigger circuit with a three-transistor amplifier on each output. The input amplifiers isolate the pulse input circuits and give high input impedance. The amplifiers give enough delay to allow the flip-flop to be set at the same time that it is being sensed. Figure 43 shows the waveforms of this flip-flop package when complemented at a 10-megapulse rate. The rise and fall times, about 25 mμsec, are faster than one normally sees in a single inverter that pulls to ground and an emitter follower that pulls to –3 volts. Figure 44 is a plot of the pulse amplitude necessary to complement the flip-flop at various frequencies. Note the independence of trigger sensitivity to pulse repetition rate. This circuit will operate at a 10-megapulse rate, twice the maximum rate at which it will be used in TX-2.

The TX-2 circuits reproduced most often were designed with a minimum number of components to achieve

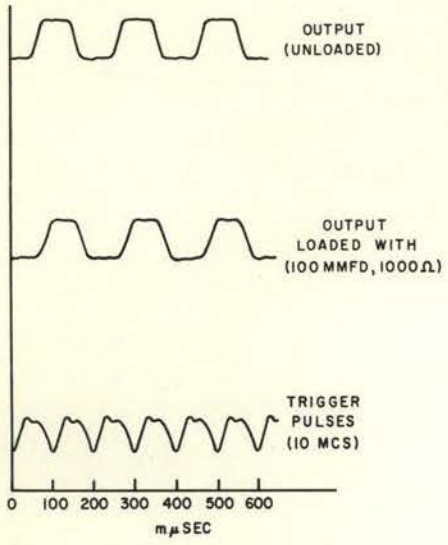

Fig. 43. Flip-flop waveforms.

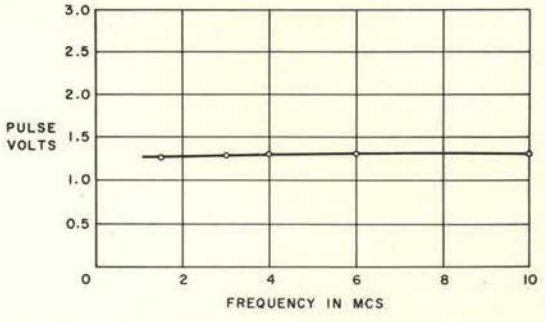

Fig. 44. Trigger sensitivity.

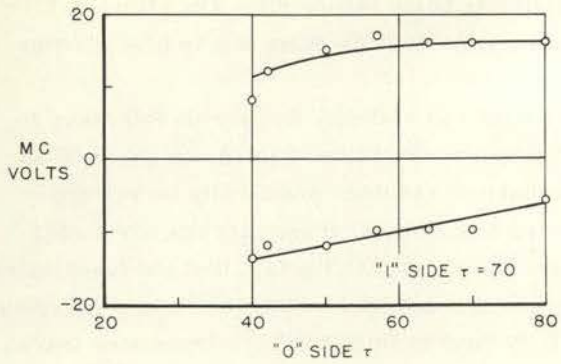

Fig. 45. τ margins.

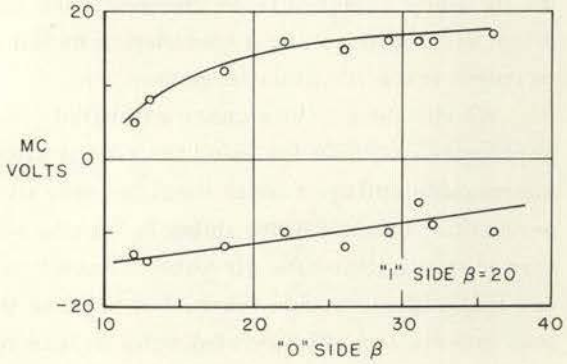

Fig. 46. β margins.

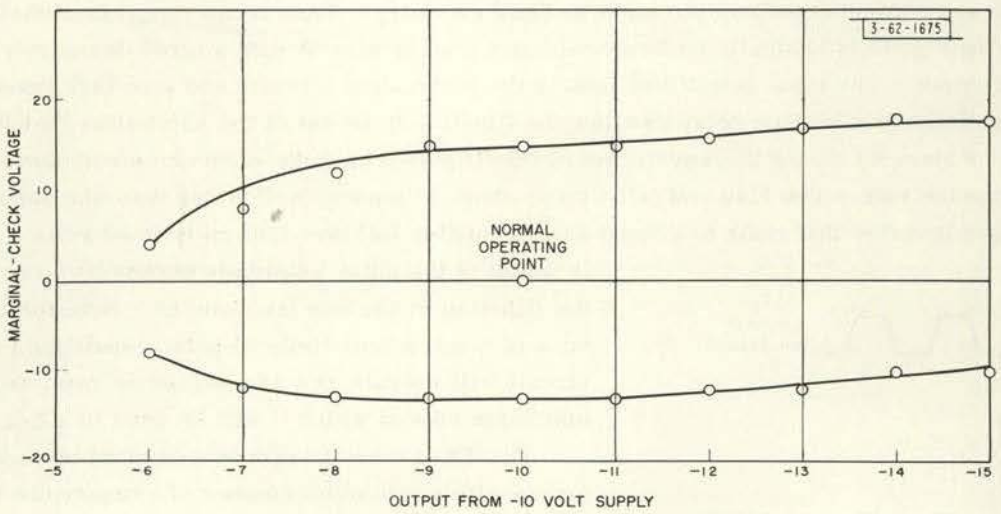

Fig. 47. −10 volt supply margins.

economies in manufacture and maintenance. The design of less frequently reproduced circuits made liberal use of components – even redundancy – to achieve long life and broad tolerance to component variations. The goal was system simplicity and high performance with a lower total number of components than might otherwise be possible. For example, the number of flip-flops in the TX-2 is small compared to the gates which transfer information from one group of flip-flops to another; so the flip-flops were allowed to be relatively complicated. But the TX-2 transfer gates were made very simple; a transfer gate is, in fact, only a single inverter. The emitter is connected to the output of the flip-flop being read and the collector is connected to the input of the flip-flop being set. The output impedance of the flip-flop is so low that, when the output is at the ground level, a pulse on the base of the transfer gate shorts the input of the other flip-flop to ground and sets its condition.

C. MARGINAL CHECKING

We planned to incorporate marginal checking in the design of these circuits so that, under a process of regularly scheduled maintenance, deteriorating components could be located before they caused failure in the system. We also found it practical to use this technique, during the design of the circuits, to locate the design center of the various parameters and to indicate the tolerance of circuit performance of these parameters. A further application of marginal checking has been found in other systems during shakedown and initial operation to pin-point noise and other system faults not serious enough to cause failure and, therefore, very difficult to isolate by other means.

The operating condition of the inverters is indicated by varying the +10-volt bias. In the flip-flop schematic in Fig. 42, the inverters were divided into two groups for marginal checking, and the two leads, labeled MCA and MCB, were varied one at a time for the most critical checking of the circuit. The curves in Figs. 43 and 44 show the locus of failure points for various parameters as a function of the marginal checking voltage. Figure 45 shows the tolerance to τ, a measure of hole storage, and Fig. 46 shows the tolerance to β, the current gain. Operating margins for supply voltages, temperature, and pulse amplitude are shown in Figs. 47 through 50.

D. PACKAGING

The number of types of plug-in units was kept small for ease of production and to keep the number of spares to a minimum. The circuits are built on dip-soldered, etched boards and the components are hand-soldered to solid turret lugs. The boards are mounted in steel shells shown in Fig. 51 to keep the boards from flexing. The male and female contacts are machined and gold-plated. The sockets are hand-wired and soldered in panels as in Fig. 52.

E. CONCLUSION

The result of these design considerations is a 5-megapulse control and arithmetic element which will take less than 40 square feet of space and dissipate less than 800 watts of power. The simplicity of the circuits has encouraged a degree of logic sophistication which would not have been chanced before.

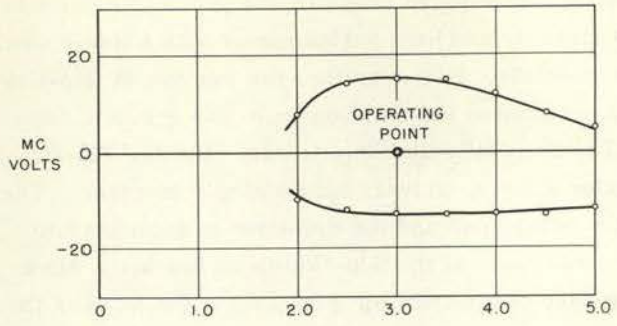

Fig. 48. −3 volt supply margins.

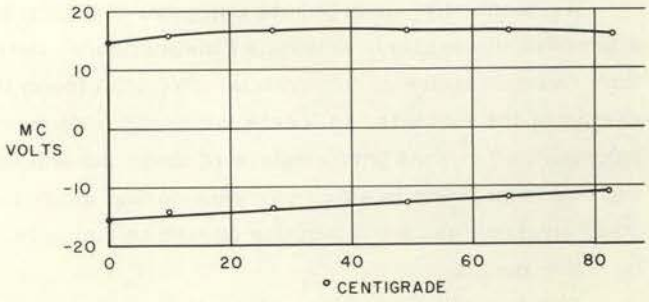

Fig. 49. Temperature margins.

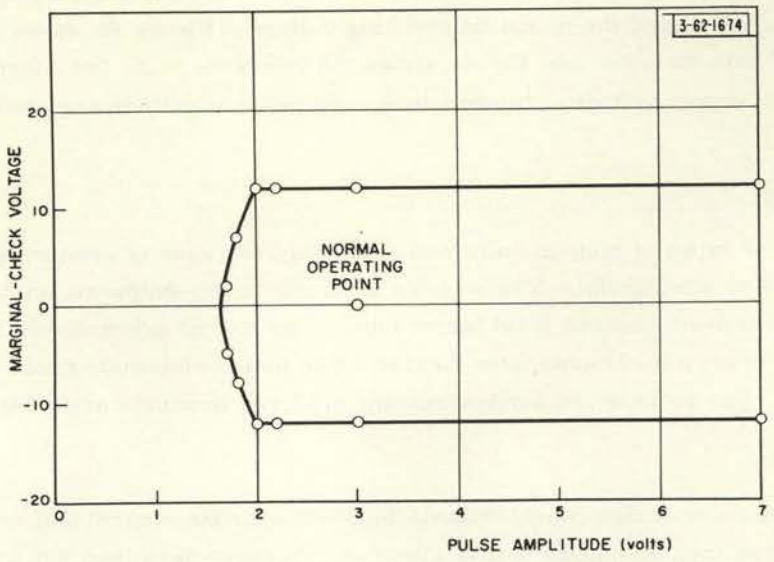

Fig. 50. Pulse margins.

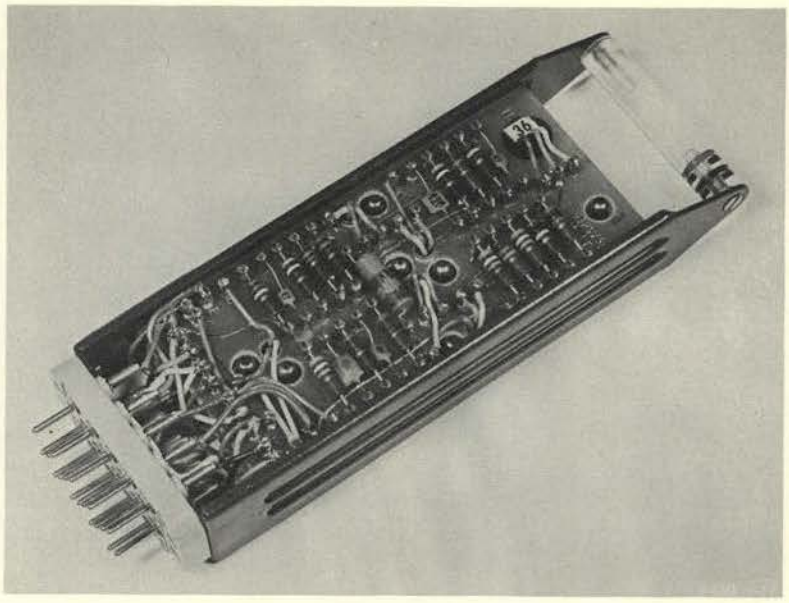

Fig. 51. TX-2 plug-in unit.

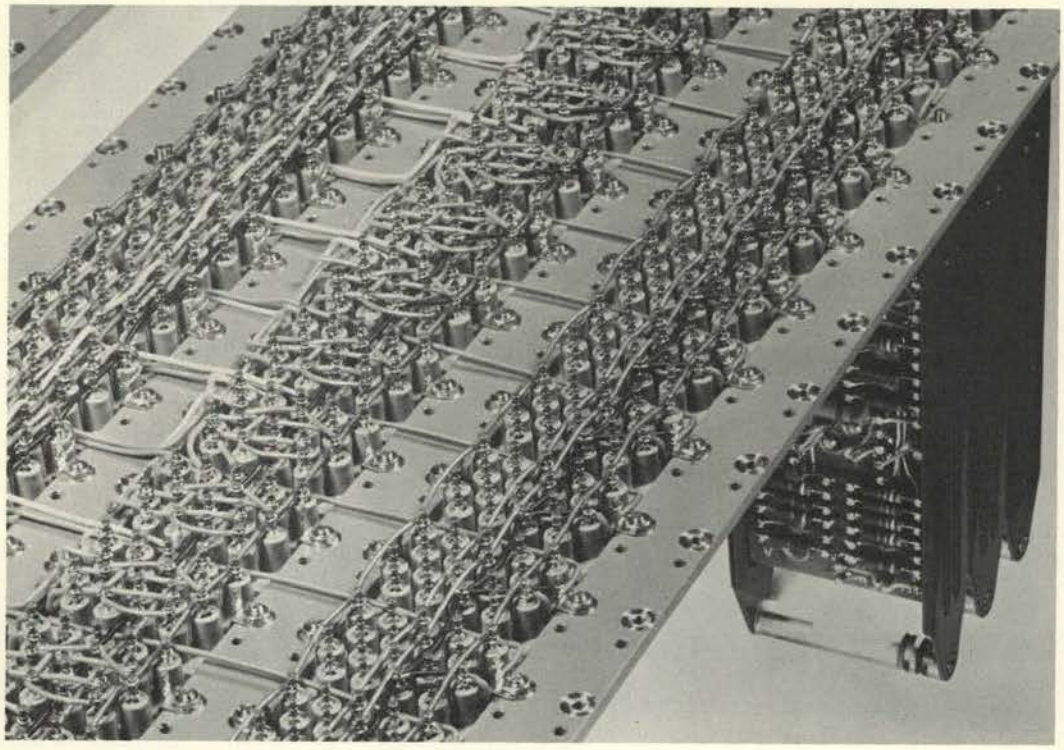

Fig. 52. TX-2 back panel.

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